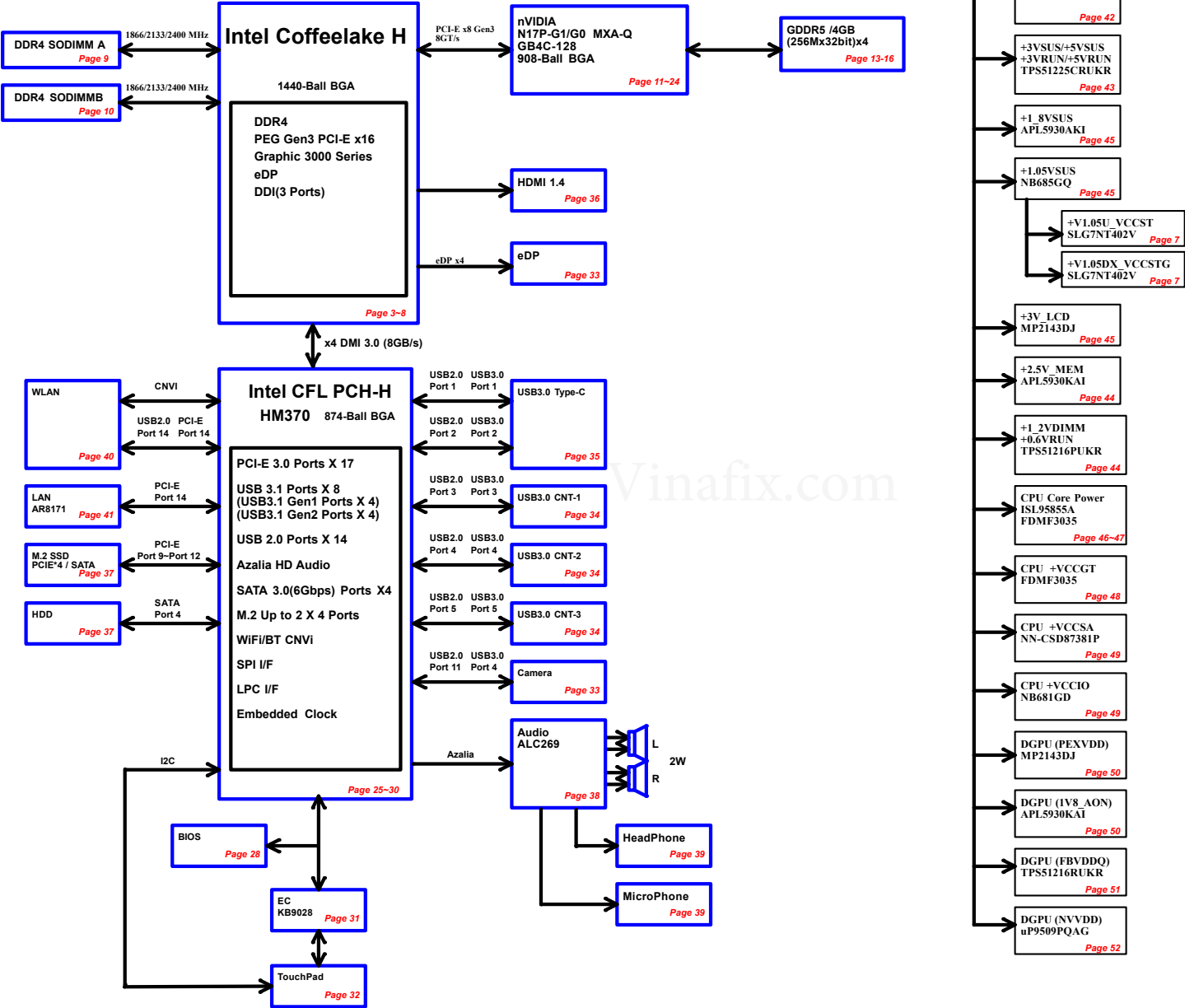
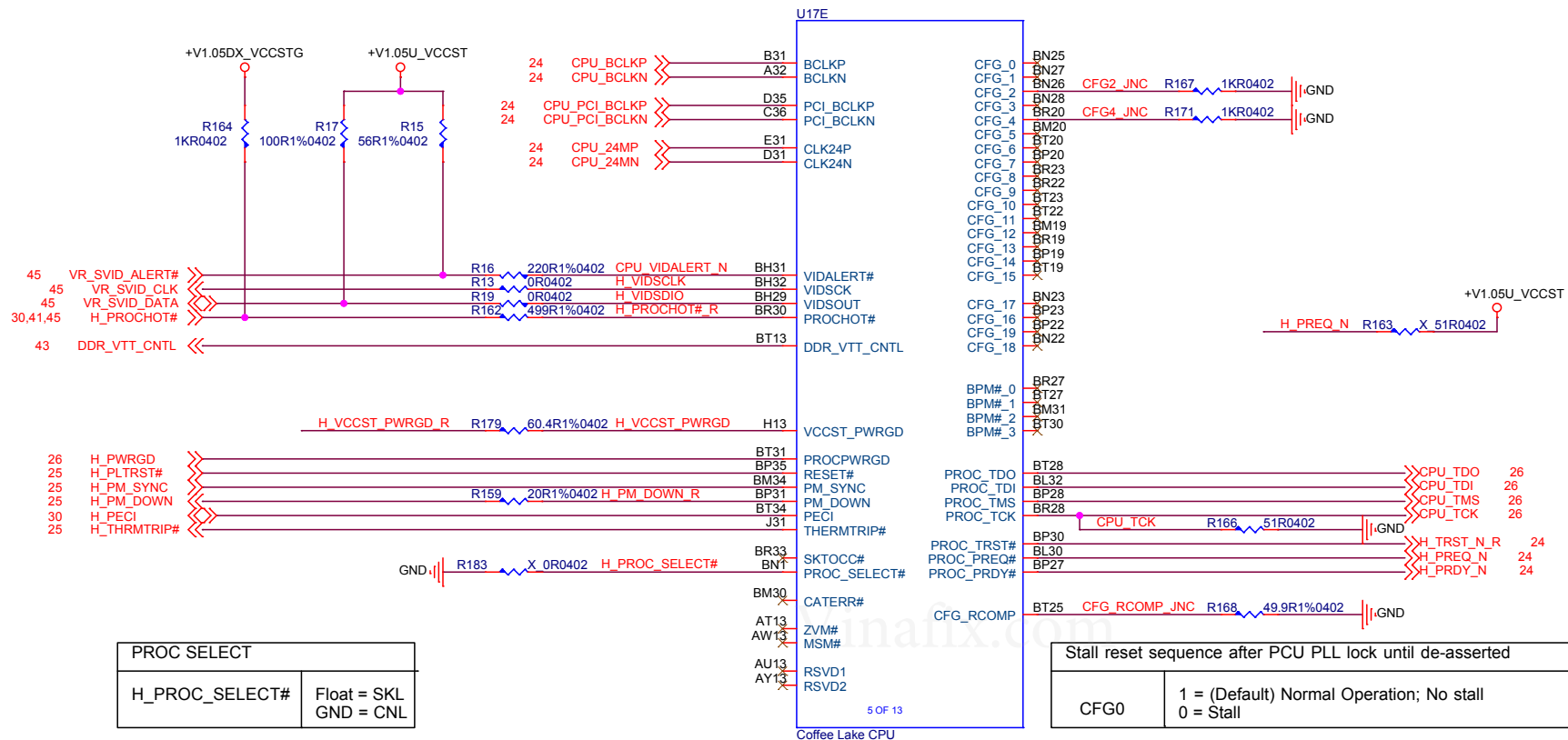
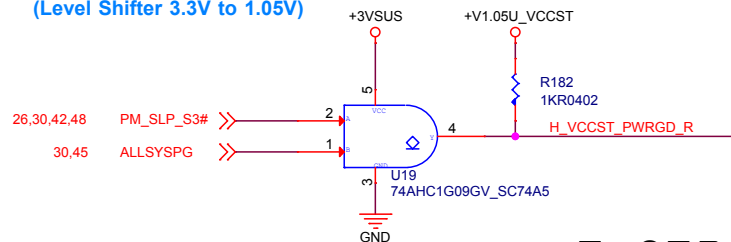






VCCST_PWRGD (Level Shifter 3.3V to 1.05V)



I7-8750H

I7_8750
A0D-8750H05-I06
X_I7-8750

I5-8300H

I5_8300
A0C-8300H05-I06
X_I5-8300

Stall reset sequence after PCU PLL lock until de-asserted

CFG0	1 = (Default) Normal Operation; No stall 0 = Stall
------	---

PCI Express * Static X16 Lane Numbering Reversal

CFG2	1 = Normal operation 0 = Lane numbers reversed.
------	--

eDP Enable

CFG4	1 = Disabled 0 = Enabled
------	-----------------------------

PCI Express* Bifurcation

CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
----------	--

PEG DEFER TRAINING

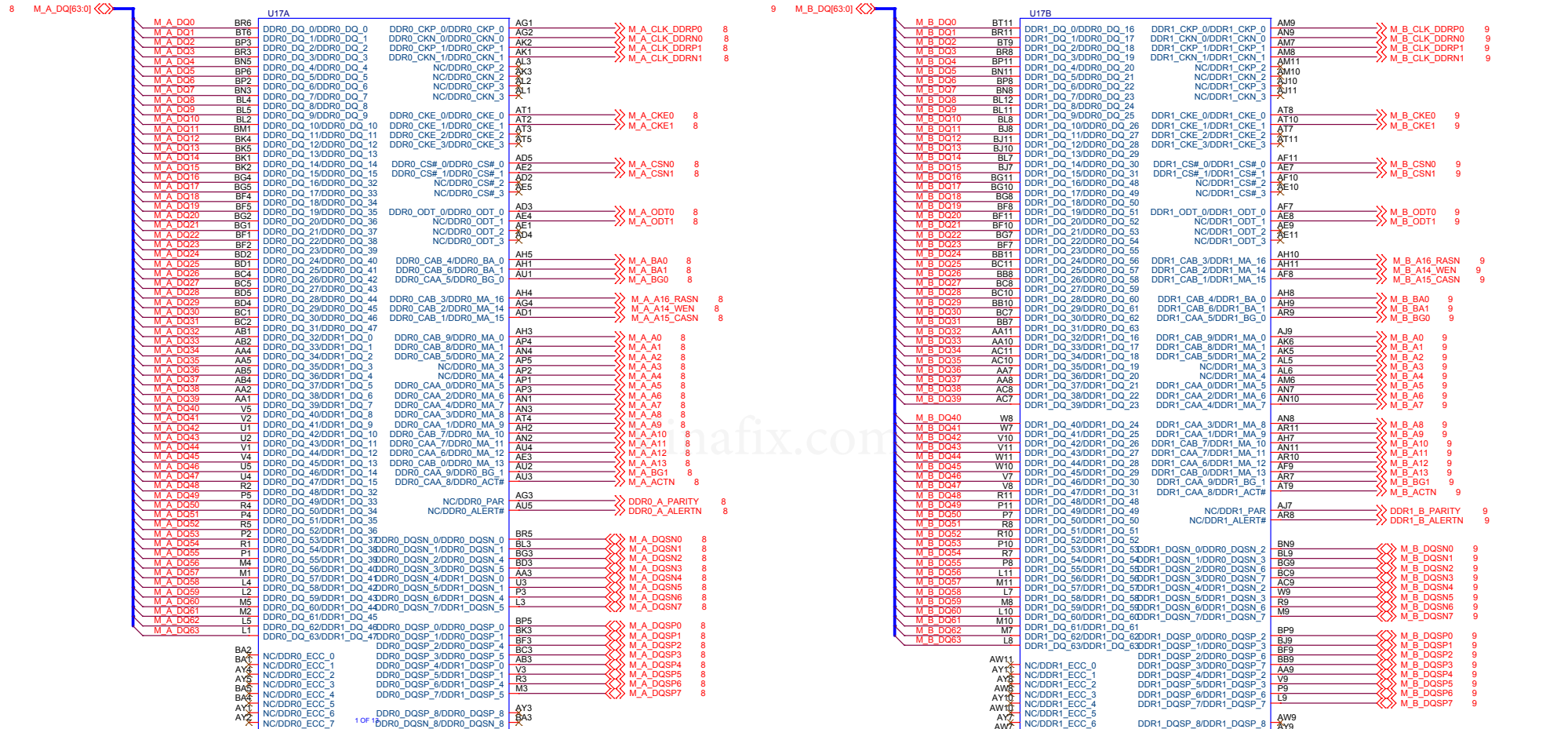
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0: PEG Wait for BIOS for training
------	--

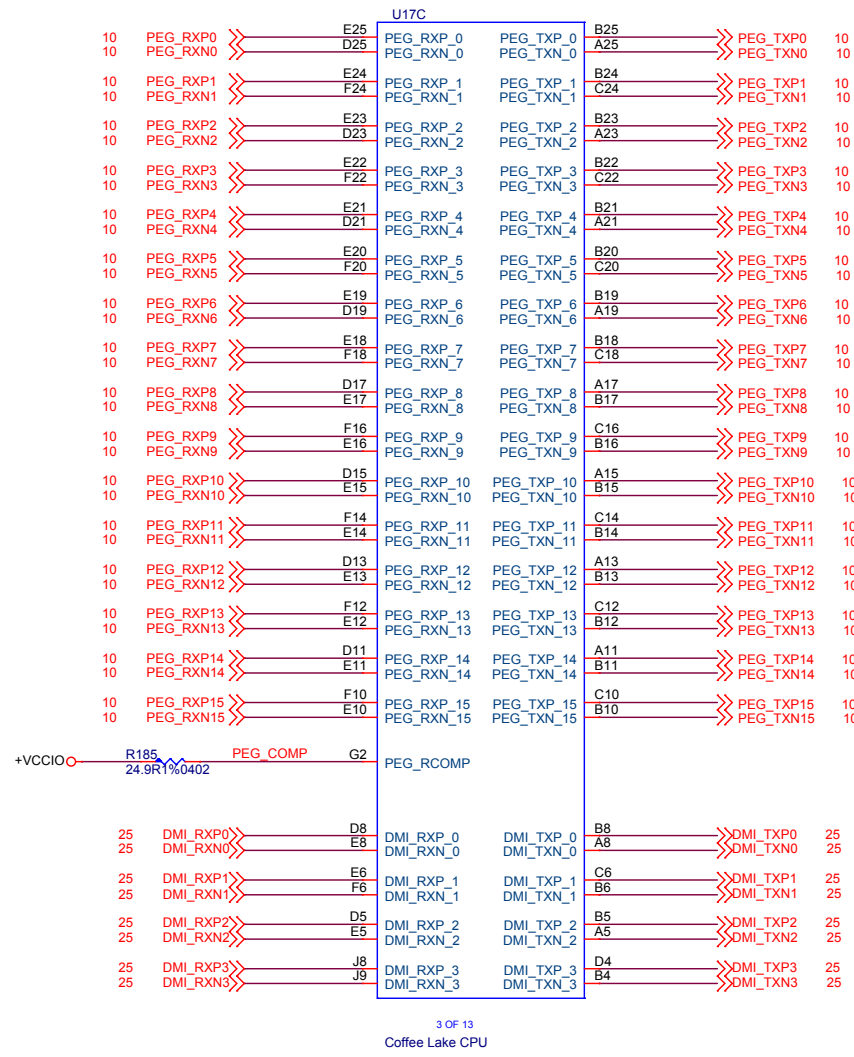
msi MICRO-STAR INT'L CO.,LTD.

Title Coffeelake(HOST)		
Size Custom	Document Number MS-16R1	Rev 1.0
Date: Wednesday, April 11, 2018 Sheet 2 of 57		

DDR Channel A

DDR Channel B

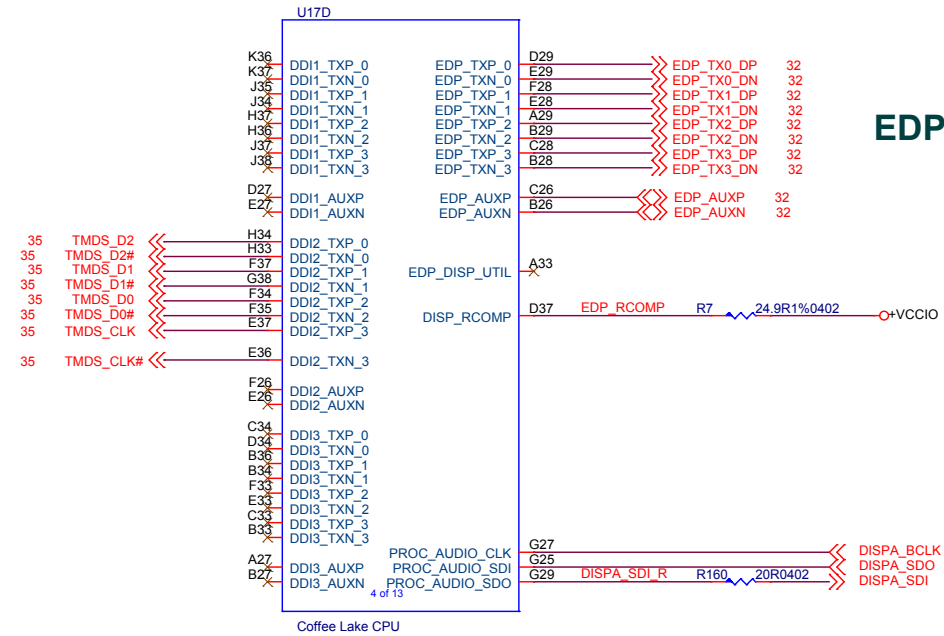




DDI C
HDMI

OUT_D0==>IN_D2
OUT_D1==>IN_D1
OUT_D2==>IN_D0

Vinafix.com

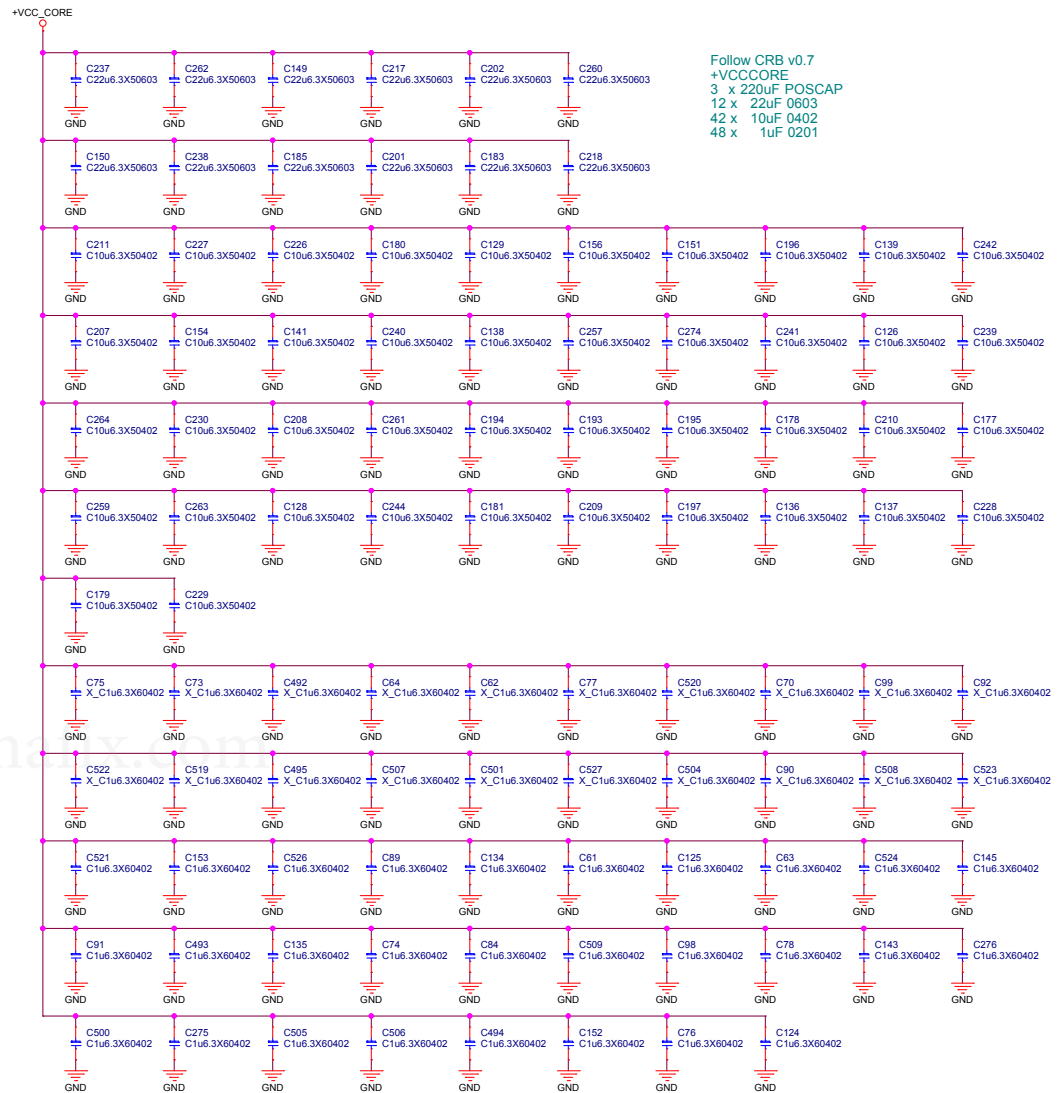
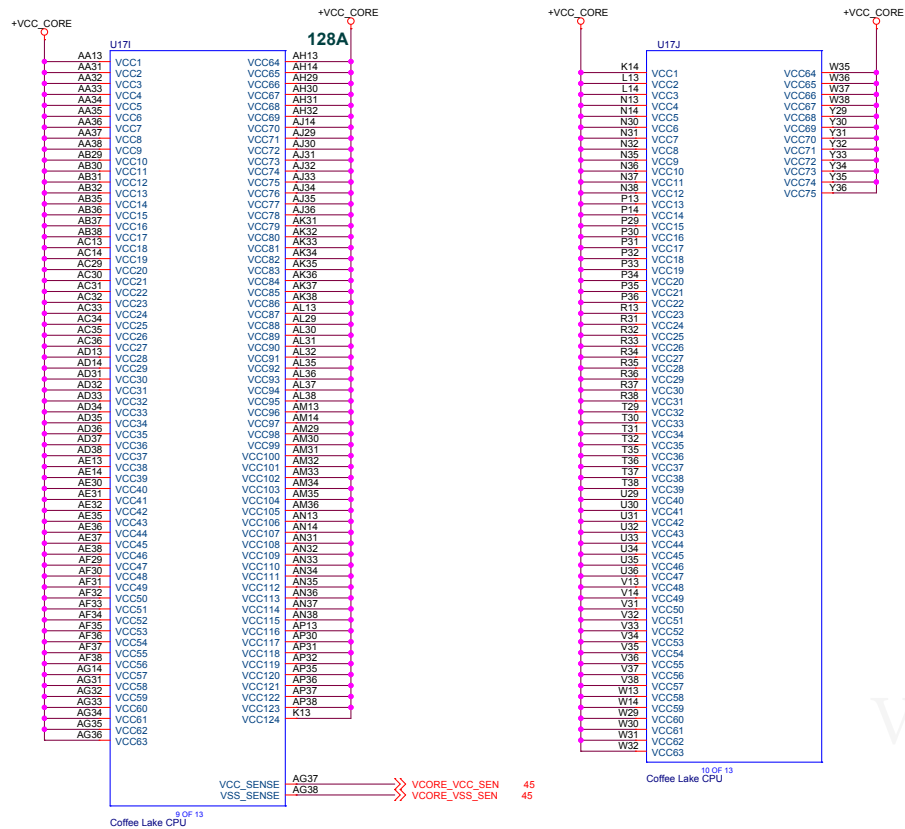


msi MICRO-STAR INT'L CO.,LTD.

Title
Coffeelake(DMI/Display)

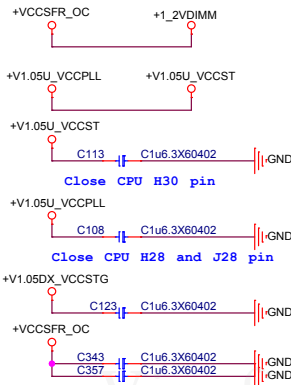
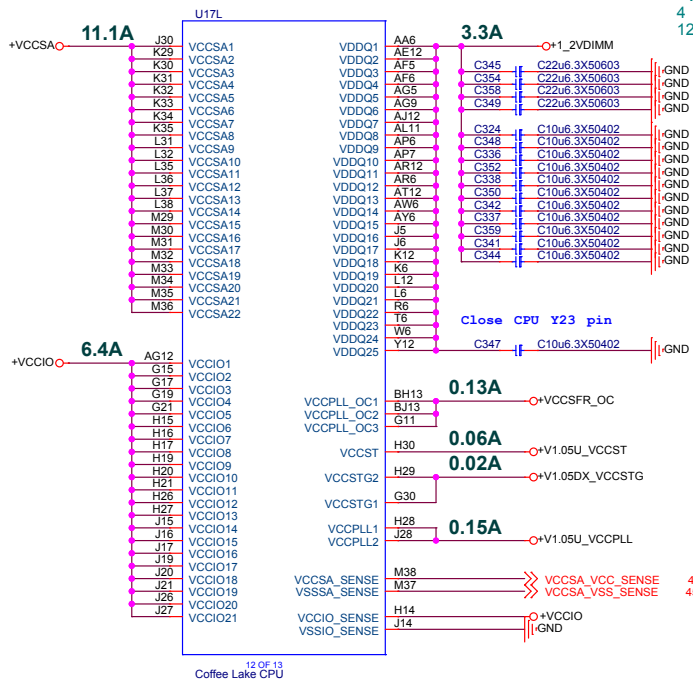
Size	Document Number	Rev
Custom	MS-16R1	1.0

Date: Wednesday, April 11, 2018 Sheet 4 of 57



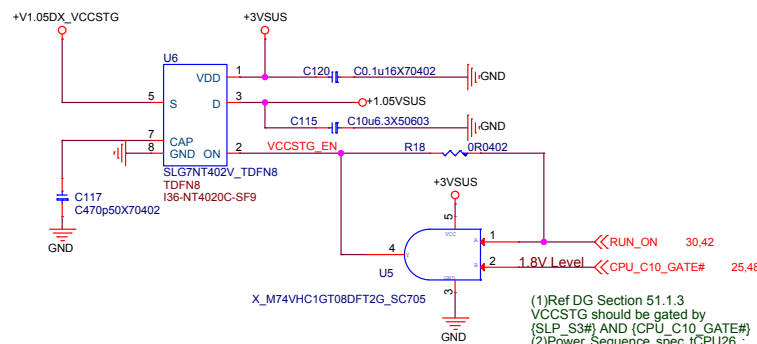
Follow CRB v0.7
+VCCCORE
3 x 220uF POSCAP
12 x 22uF 0603
42 x 10uF 0402
48 x 1uF 0201

Follow CRB v0.7
+VCCDU (+1.2VDIMM)
4 x 22uF 0603
12 x 10uF 0402



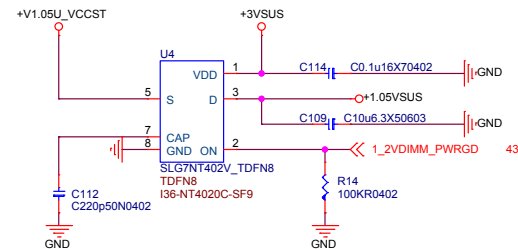
VCCST must always ramp with
or earlier then VCCSTG;

+V1.05DX_VCCSTG



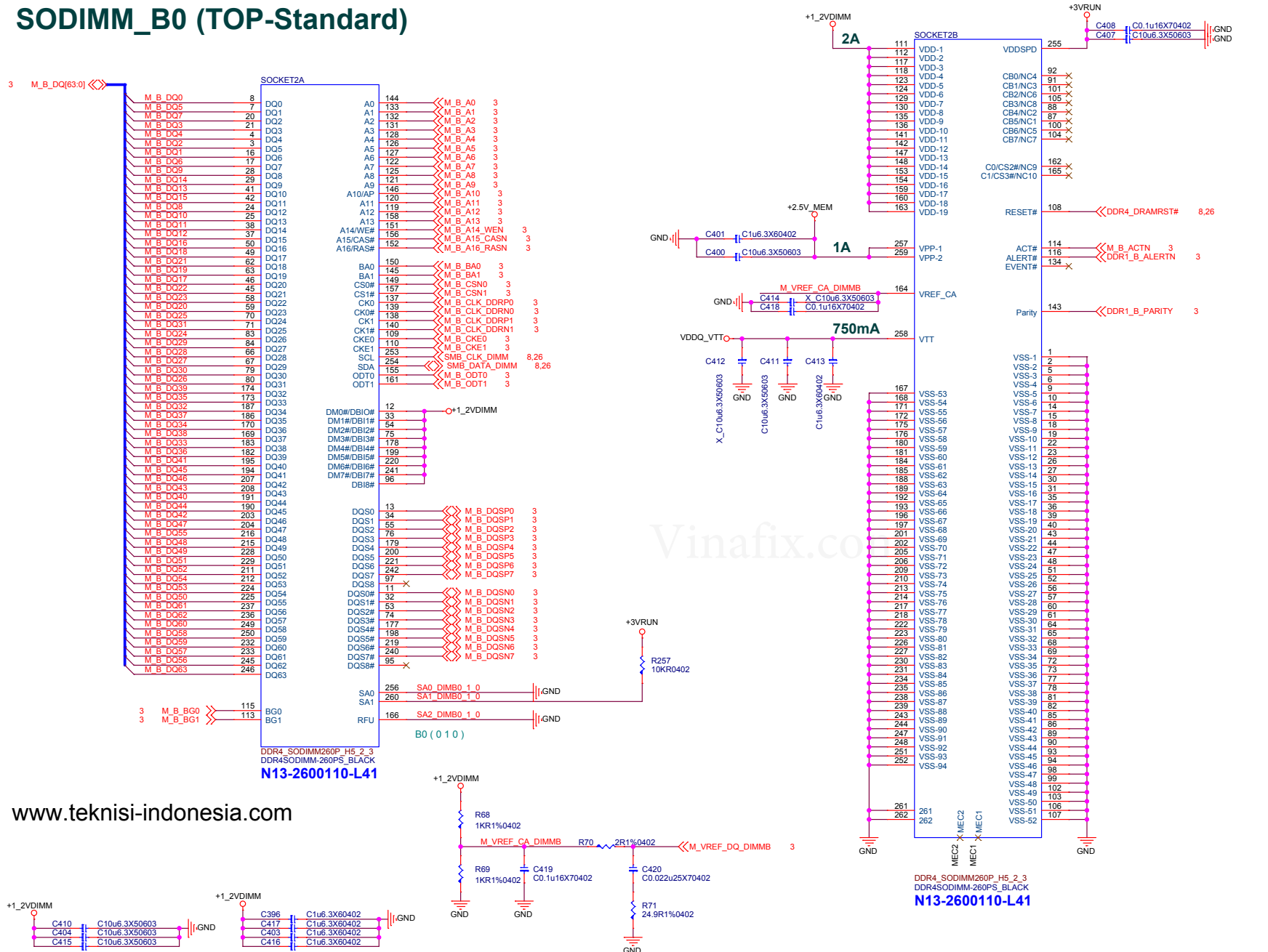
(1)Ref DG Section 51.1.3
VCCSTG should be gated by
(SLP_S3#) AND (CPU_C10_GATE#)
(2)Power Sequence spec iCPU26
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us

+V1.05U_VCCST



msi MICRO-STAR INT'L CO.,LTD.			
Title			
CoffeeLake(Power2)			
Size	Document Number	Rev	
Custom	MS-16R1	1.0	
Date:	Wednesday, April 11, 2018	Sheet	6 of 57

SODIMM_B0 (TOP-Standard)



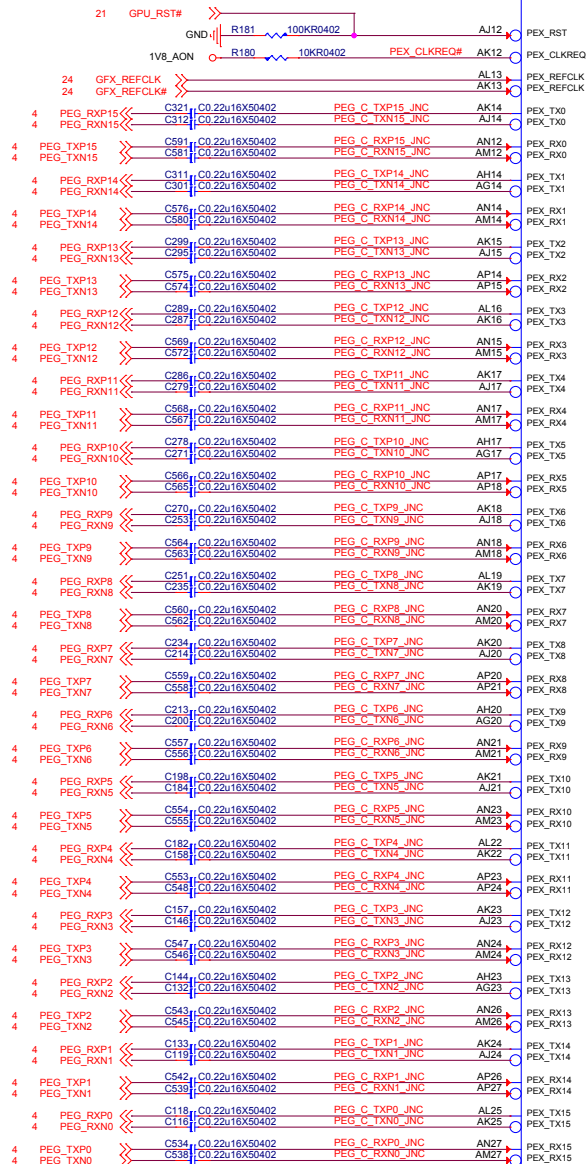
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msi MICRO-STAR INT'L CO.,LTD.	
Title DDR4 SODIMM_B0	
Size Custom	Document Number MS-16R1
Date: Wednesday, April 11, 2018	Rev 1.0
Sheet 9 of 57	

GPU PCI EXPRESS

G1A
IN155376B39
COMMON

1/17 PCI_EXPRESS

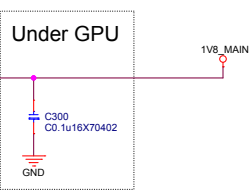
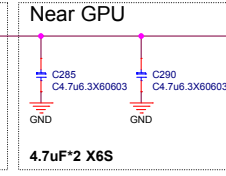
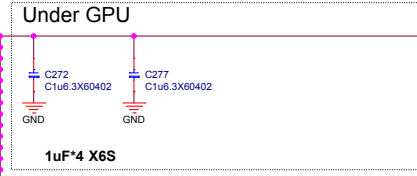
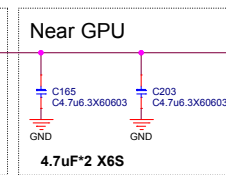
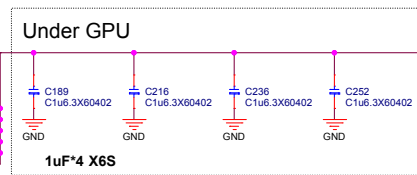


PEX_DVDD
AG19
AG21
AG22
AG24
AH21
AH25

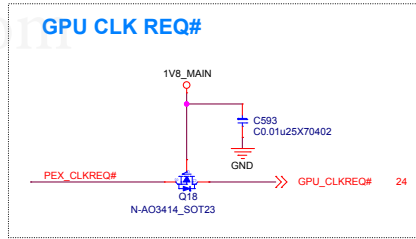
PEX_HVDD
AG13
AG15
AG16
AG18
AG25
AH15
AH18
AH26
AH27
AJ27
AK27
AL27
AM28
AN28

PEX_PLL_HVDD

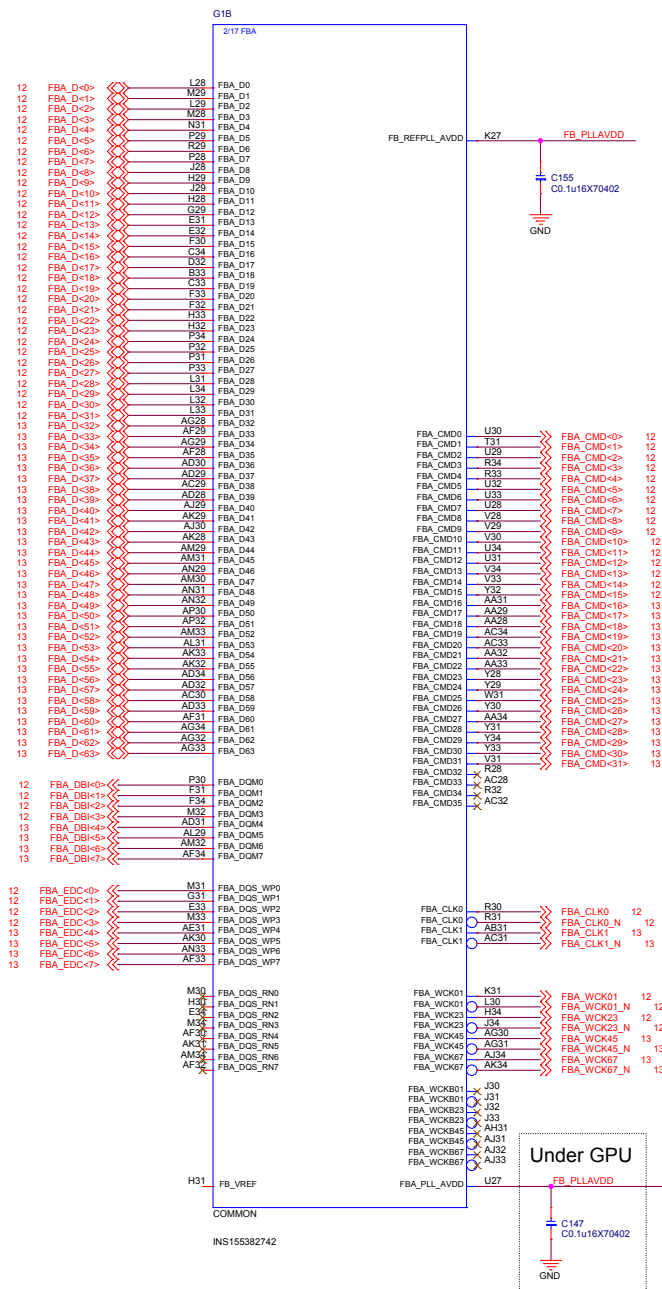
PEX_TERM



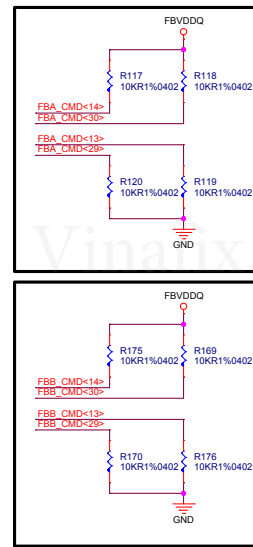
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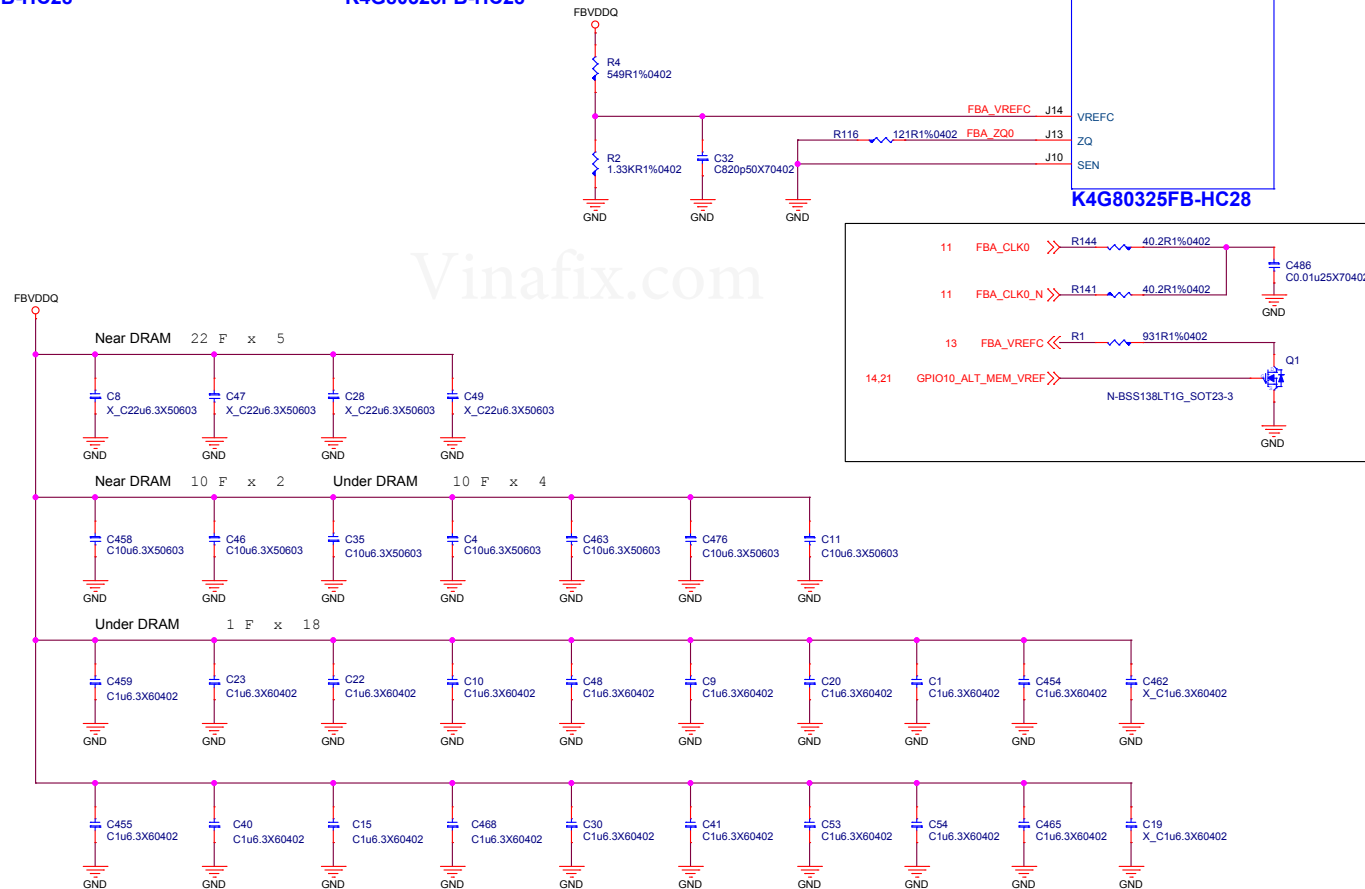
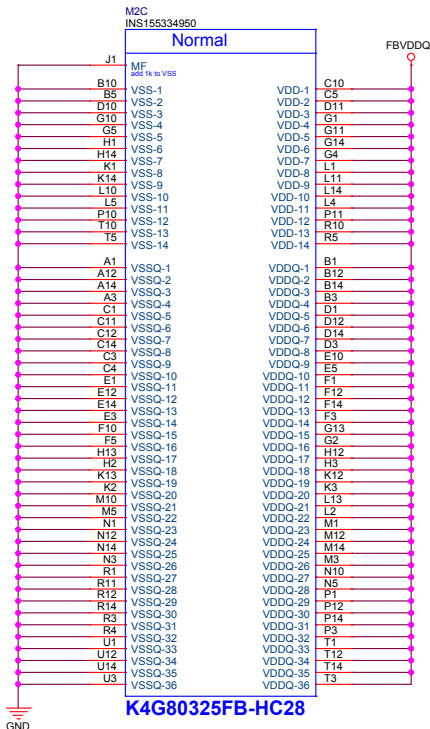
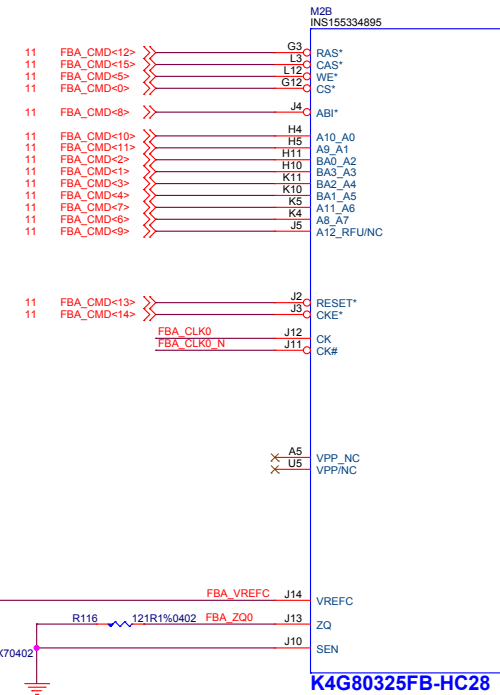
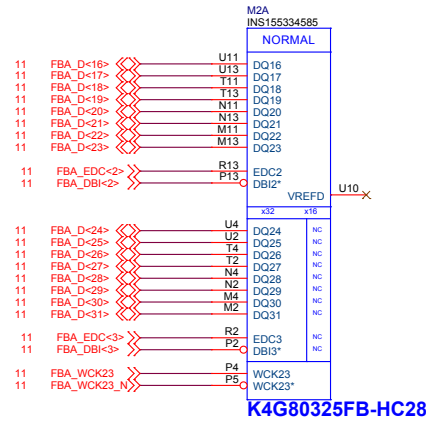
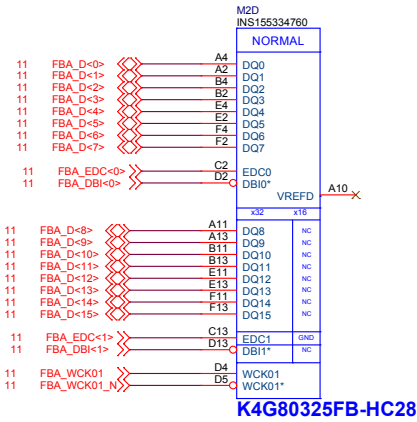
GPU Frame Buffer Partition A/B

GDD5 Command Mapping GB4C-128

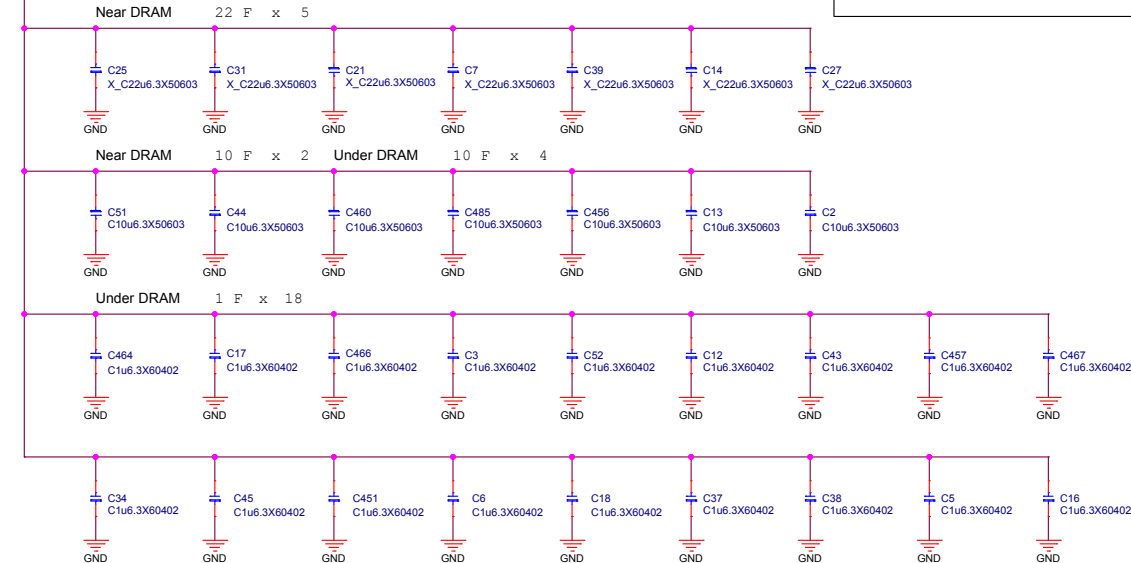
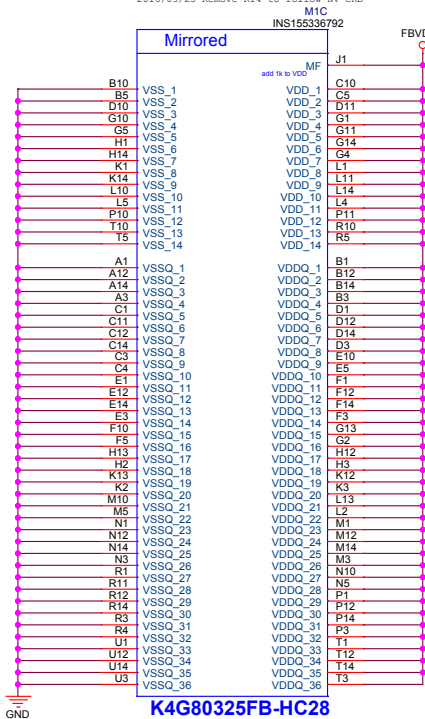
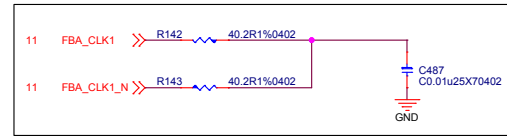
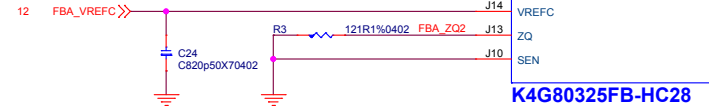
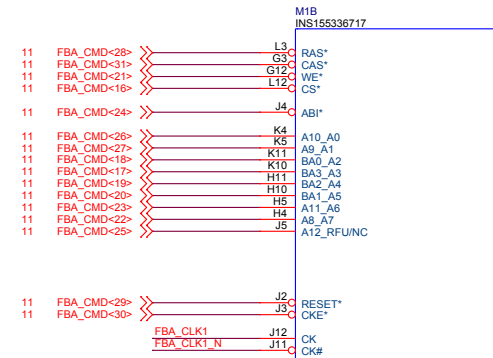
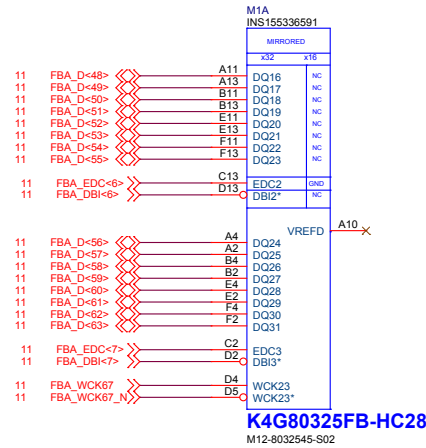
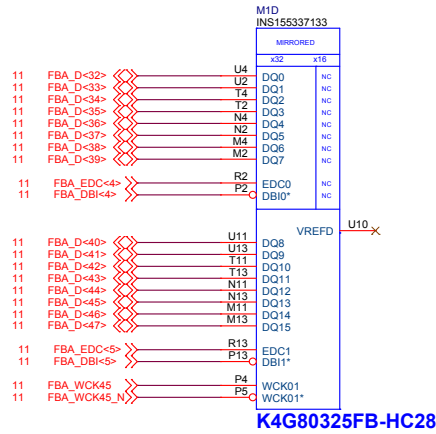
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3 BA3
CMD2	CMD18	A2 BA0
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7 A8
CMD7	CMD23	A6 A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12 RFU
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



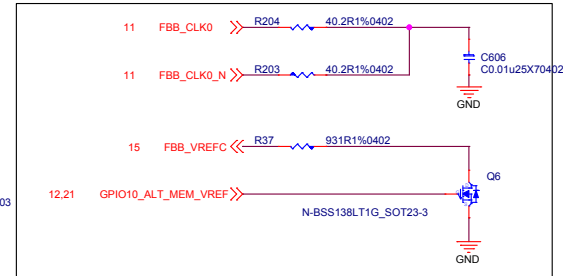
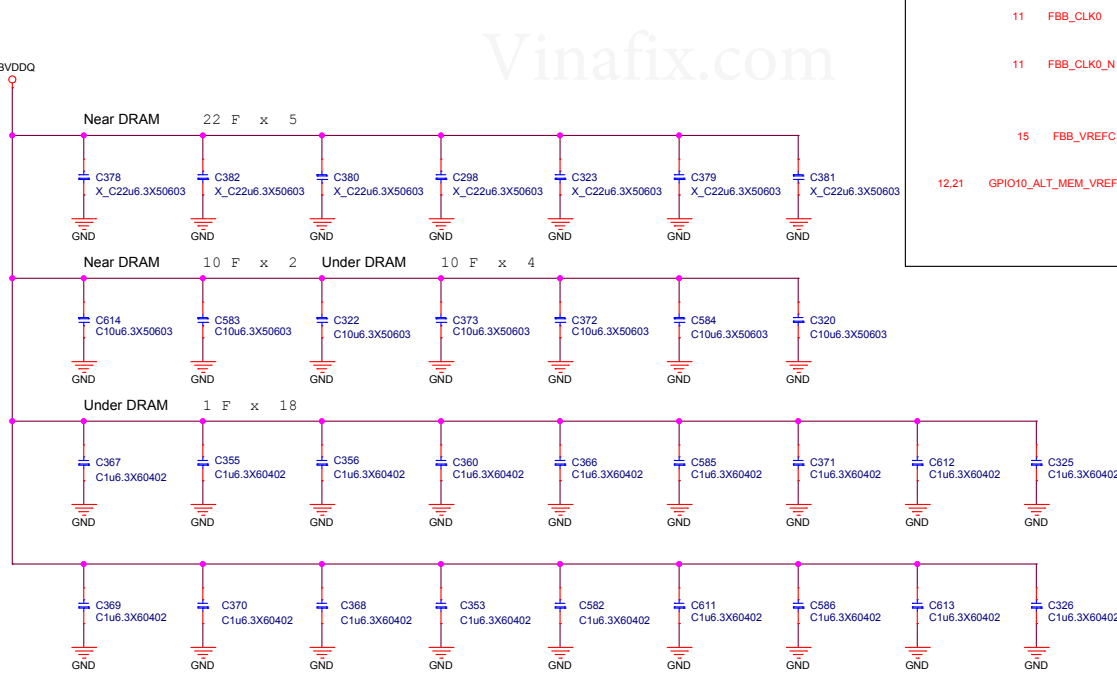
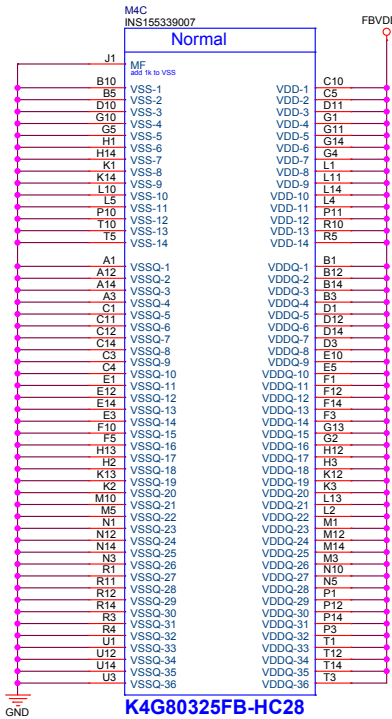
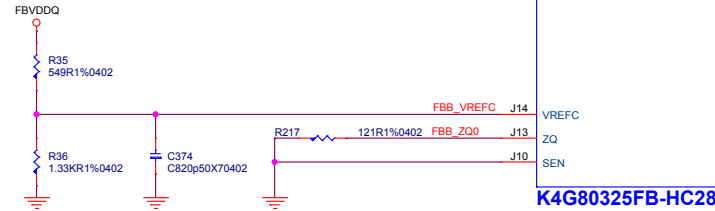
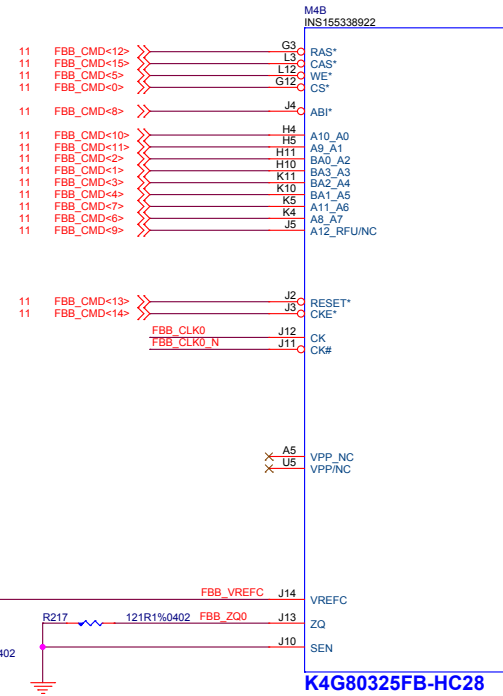
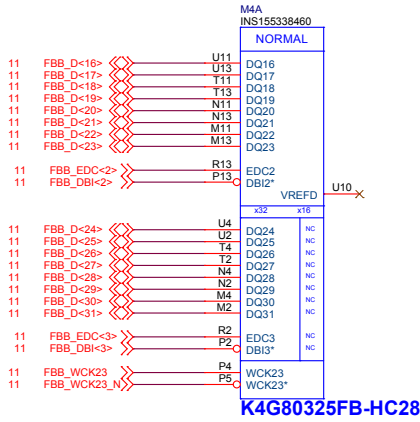
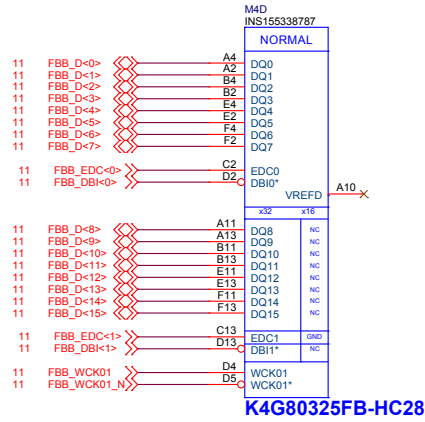
DGPU_GDDR5 FrameBuffer A0



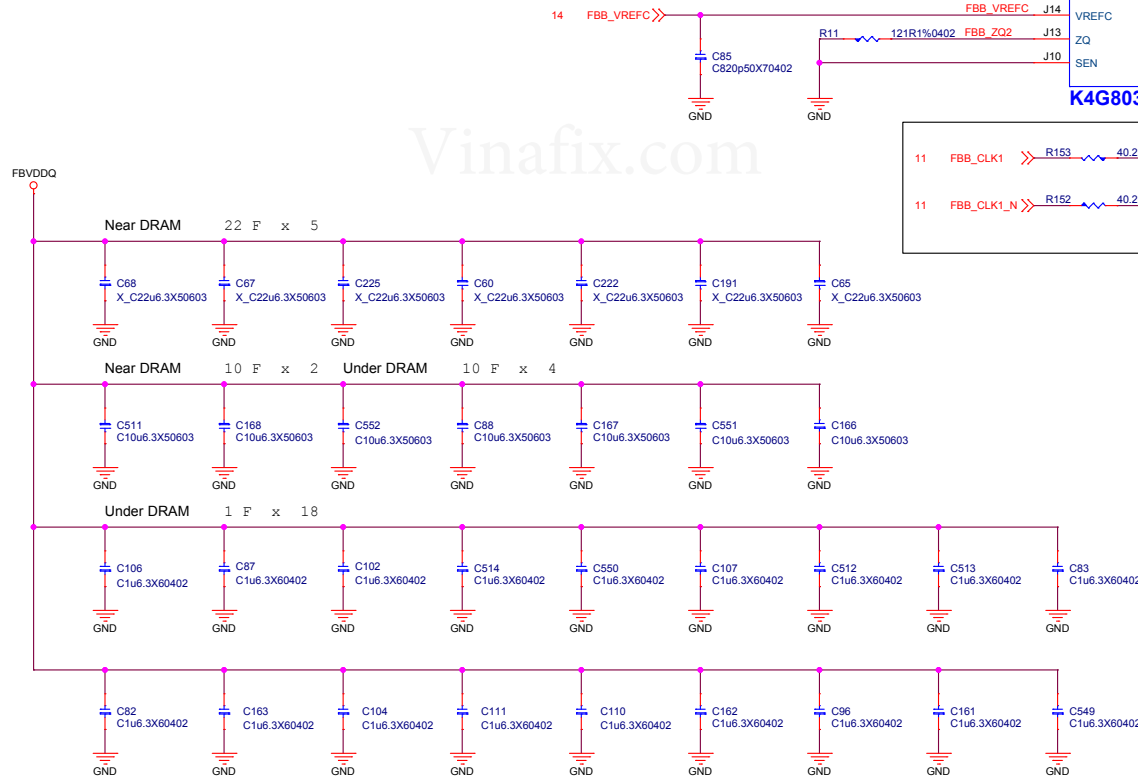
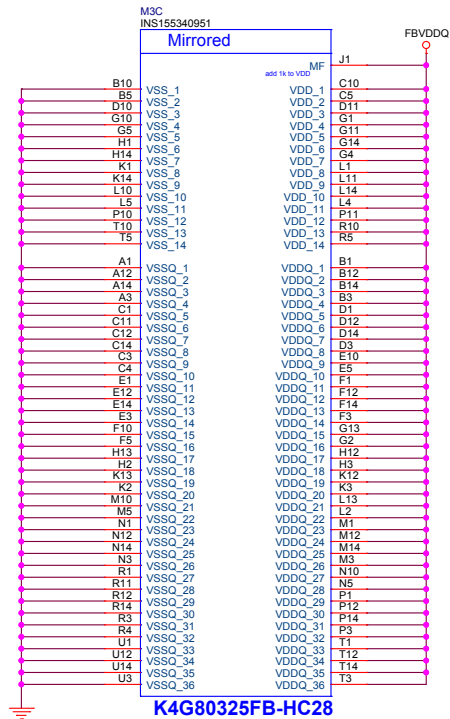
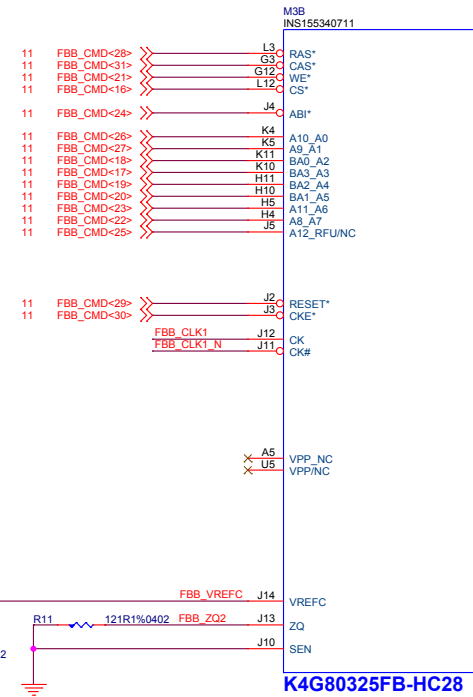
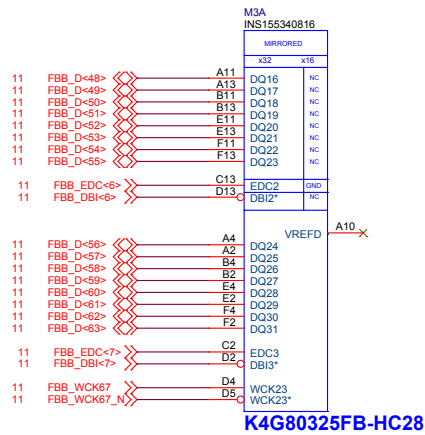
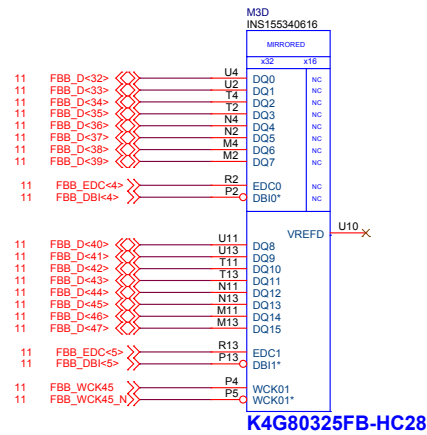
DGPU_GDDR5 FrameBuffer A1



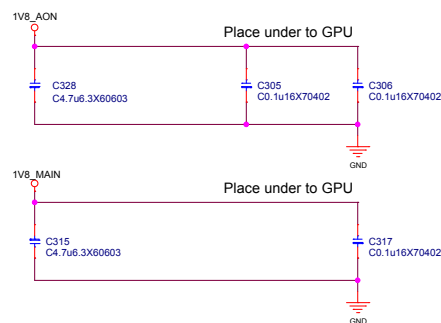
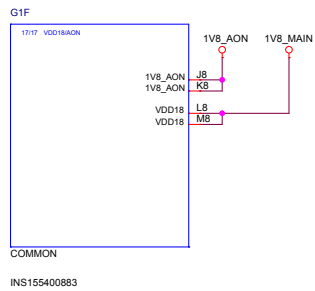
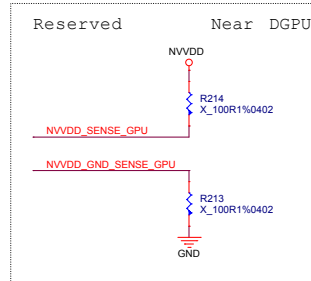
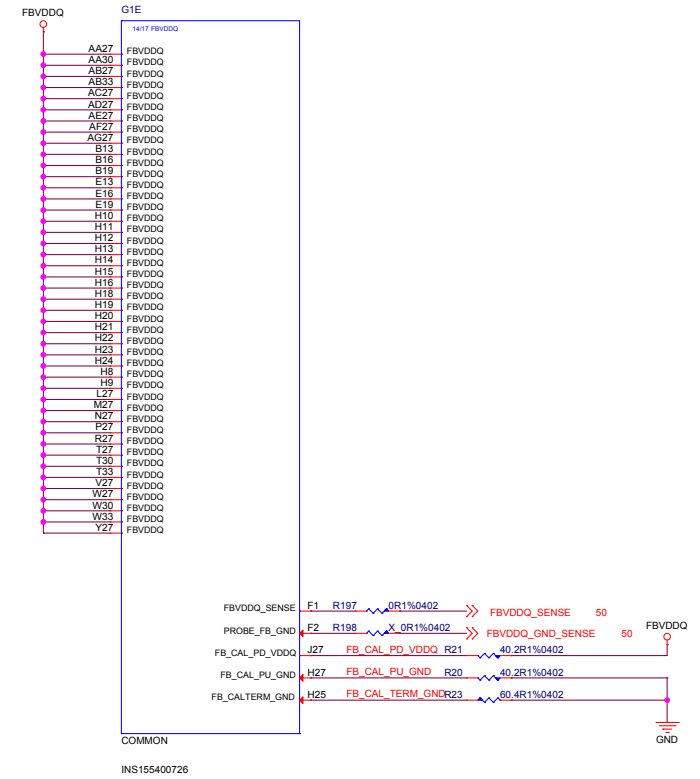
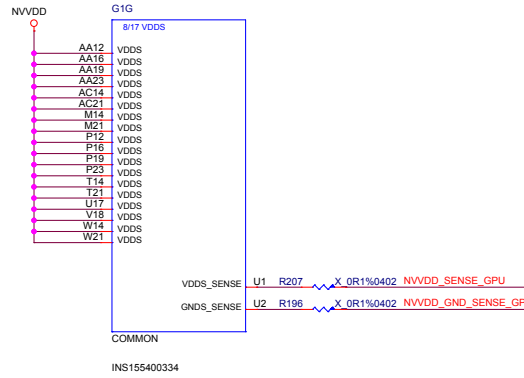
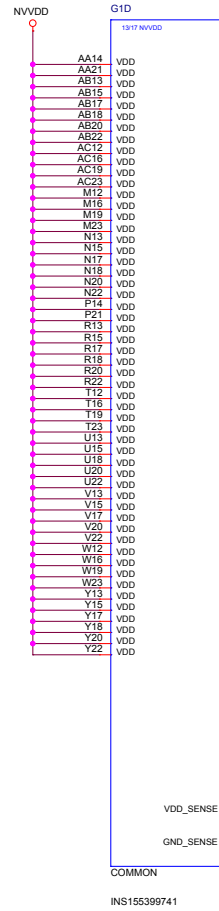
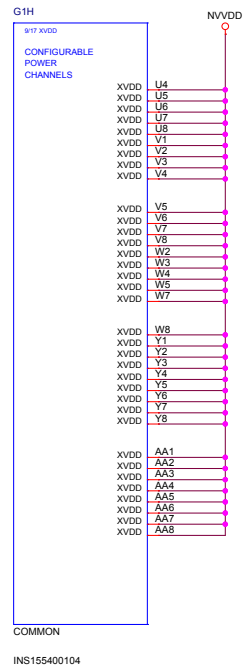
DGPU_GDDR5 FrameBuffer B0



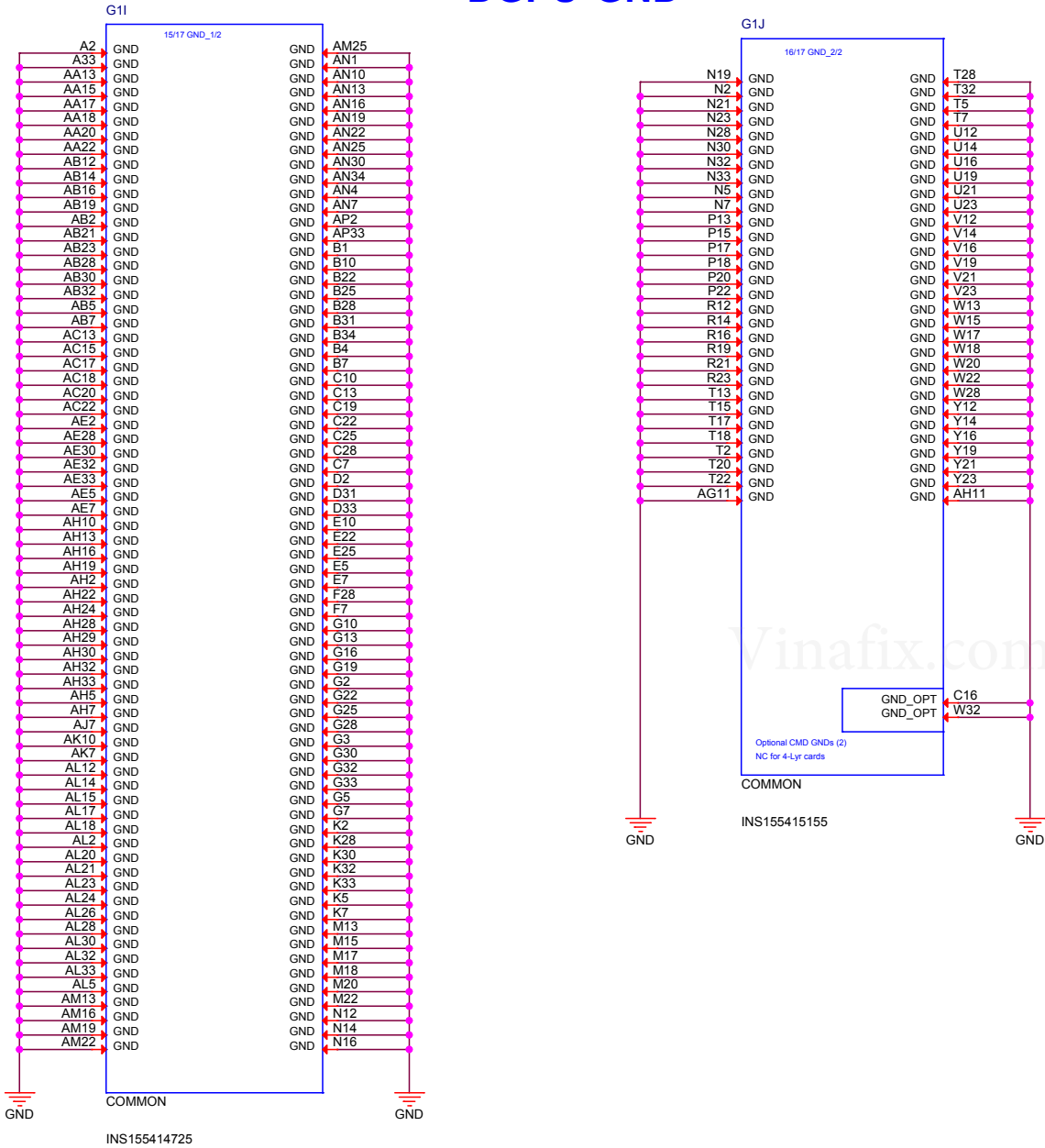
DGPU_GDDR5 FrameBuffer B1



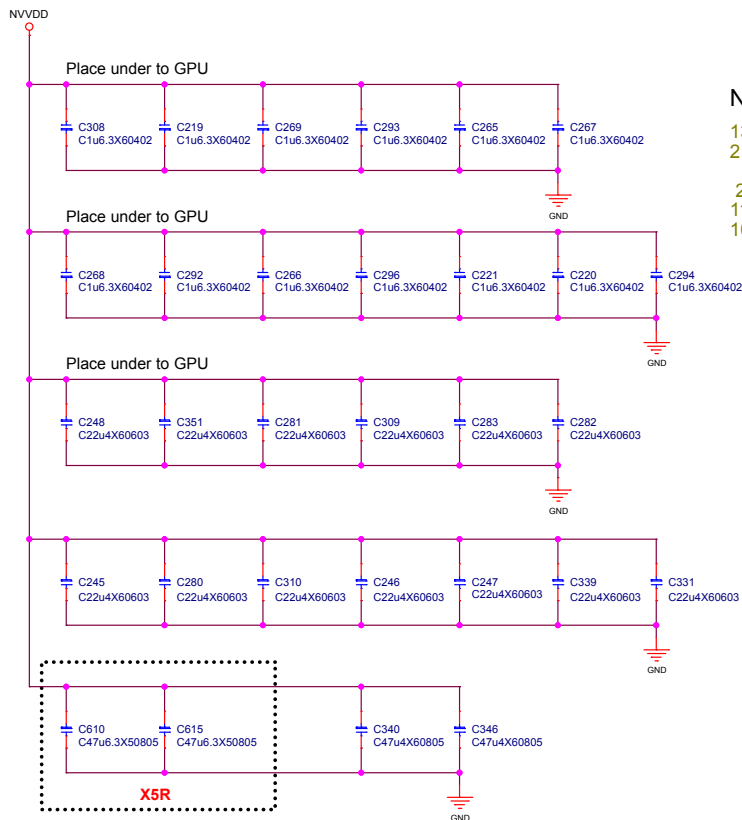
GPU NVVDD, FBVDDQ



DGPU GND



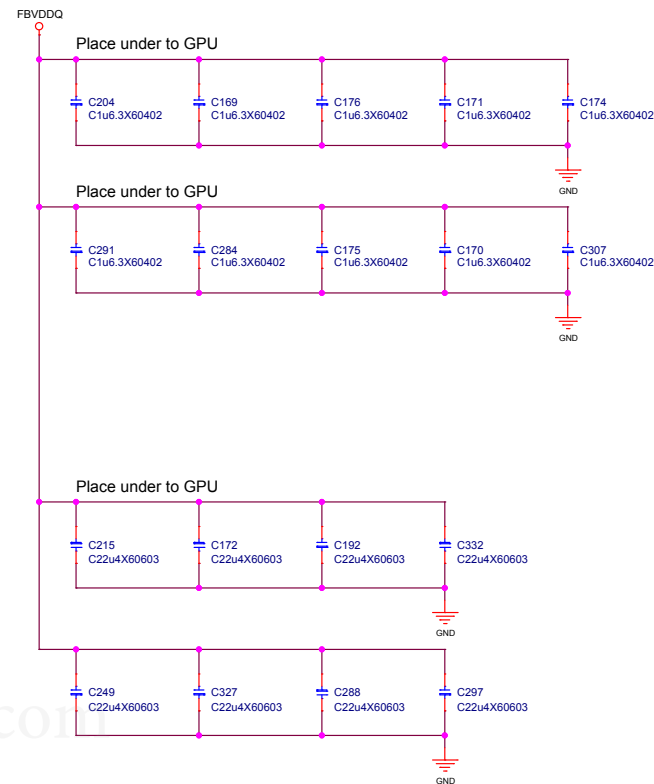
GPU DECOUPLING



NVVDD+NVDDS

13 x 1uF(Under GPU)
21 x 10uF(Under GPU)

2 x 4.7uF(Near GPU)
11 x 10uF(Near GPU)
10 x 22uF(Near GPU)



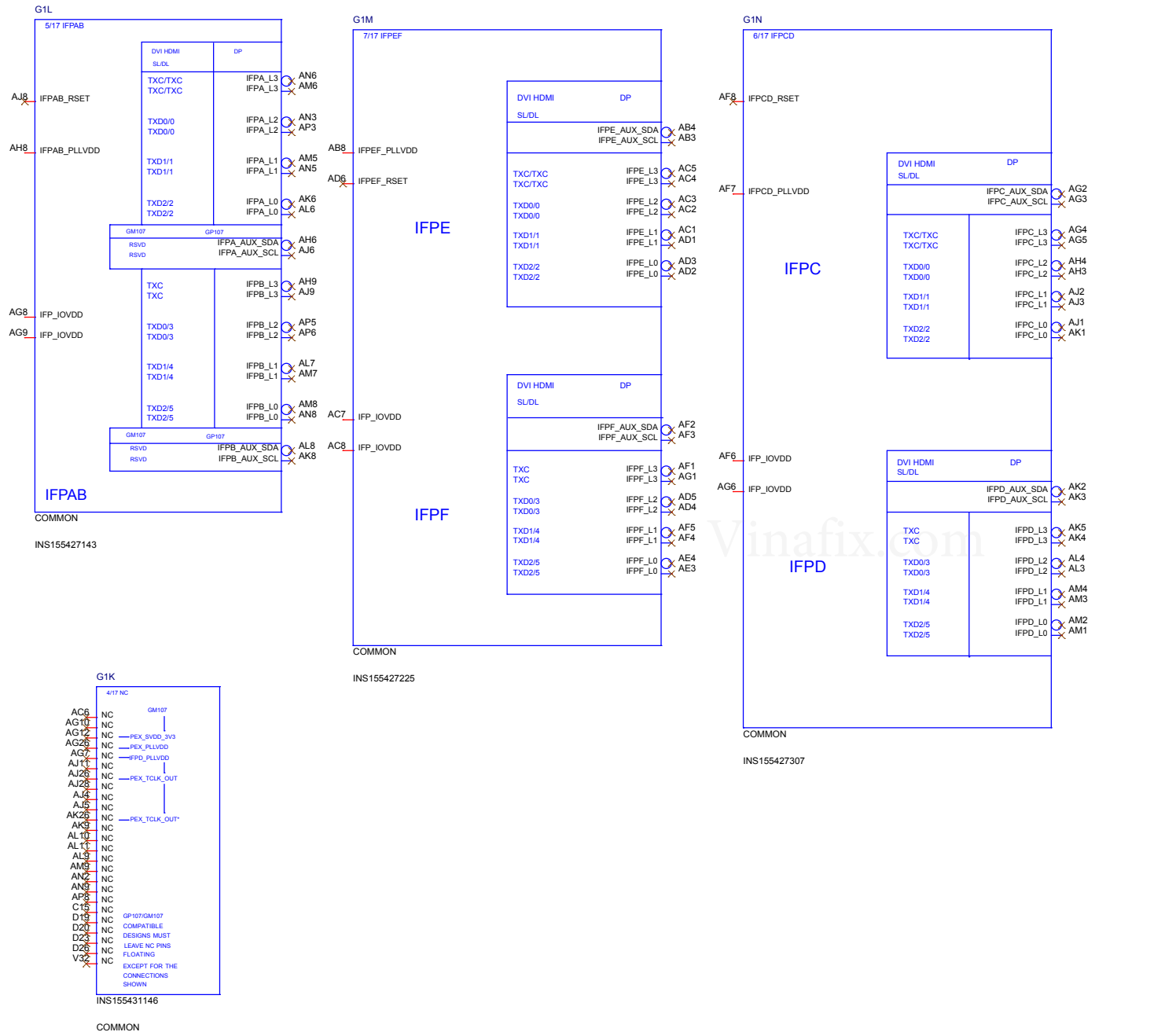
FBVDDQ

12 x 1uF(Under GPU)
4 x 10uF(Under GPU)

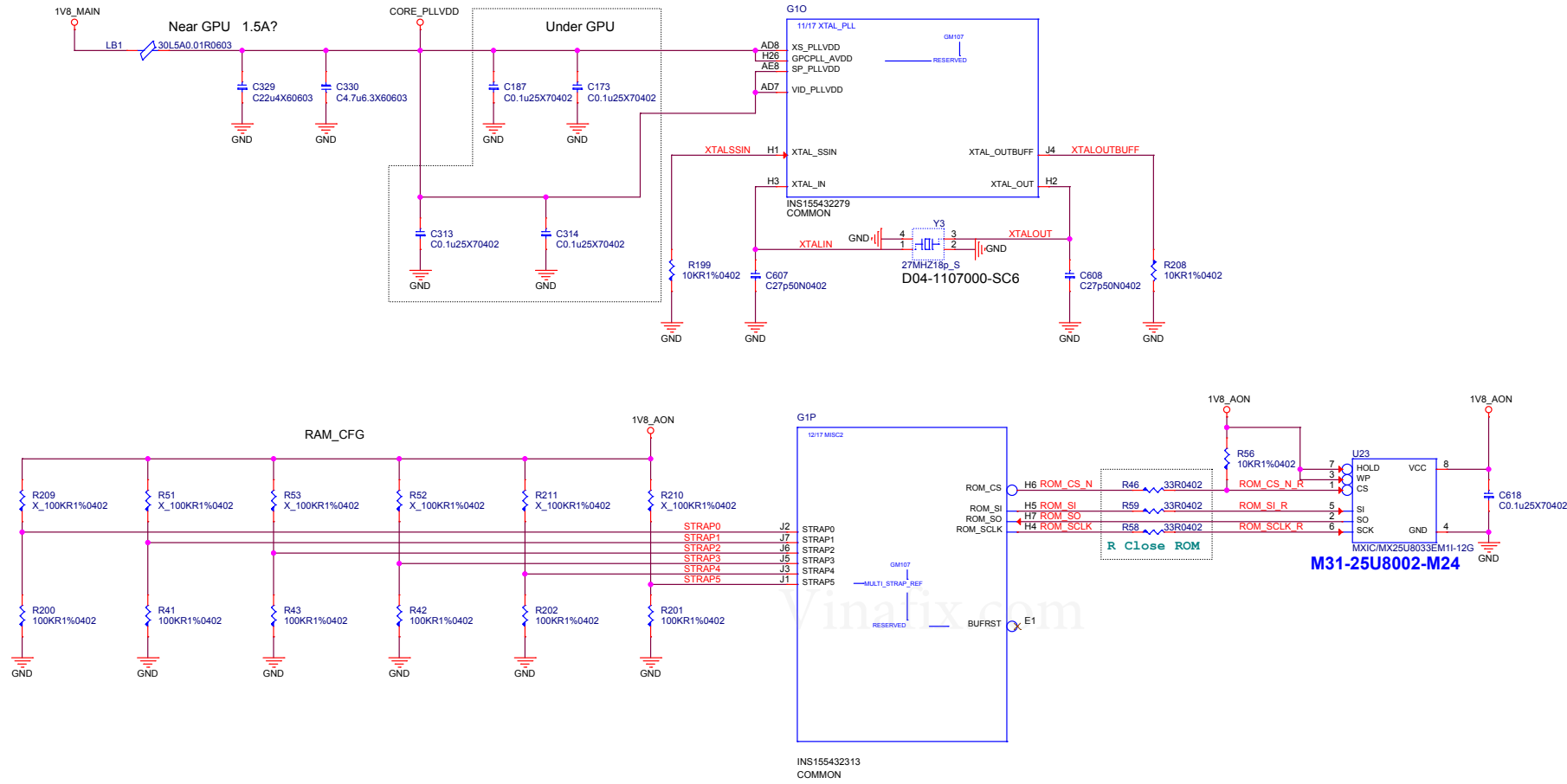
2 x 10uF(Near GPU)
5 x 22uF(Near GPU)

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DACA,Display IF



ROM, MULTI-LEVEL STRAPS

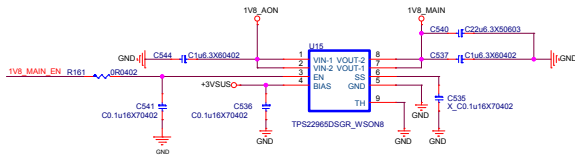


STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

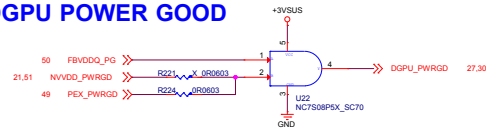
STRAP 2	STRAP 1	STRAP 0		
L	L	L	0x0	Samsung K4G80325FB-HC25
L	L	L	0x0	Samsung K4G80325FB-HC28
L	L	H	0x1	Microm MT51J2256M32HF-80:A
L	H	L	0x2	Hynix H5GC8H24MJR-R4C
H	H	L	0x6	Hynix H5GQ4H24AJR-R4C
H	H	H	0x7	Samsung K4G41325FE-HC25

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

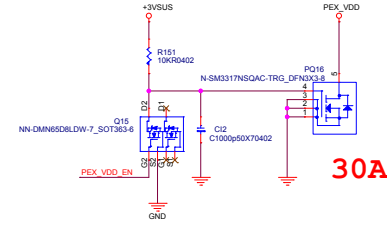
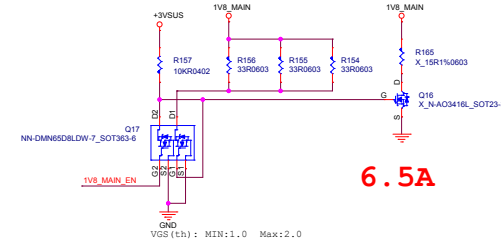
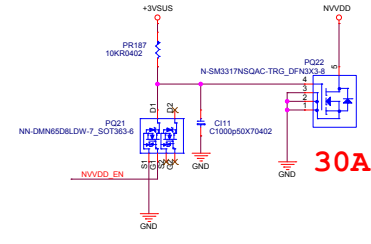
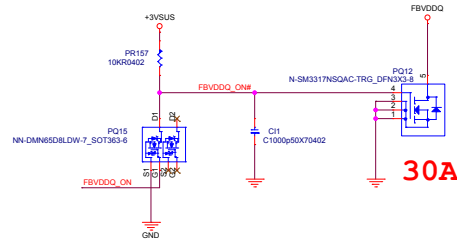
1V8_MAIN



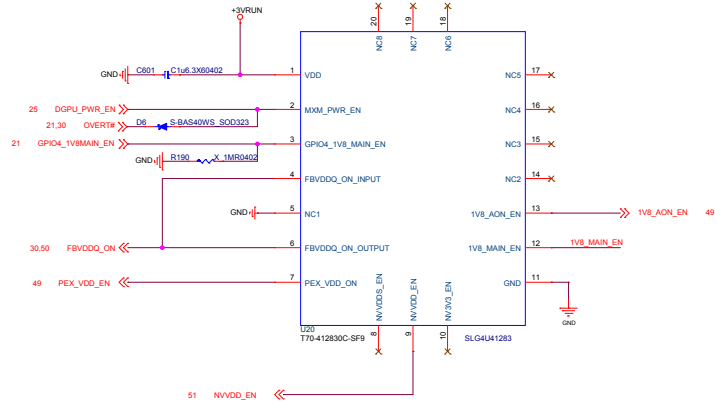
DGPU POWER GOOD



Discharge

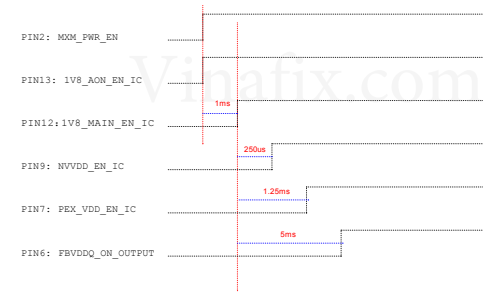


Power Sequence Control

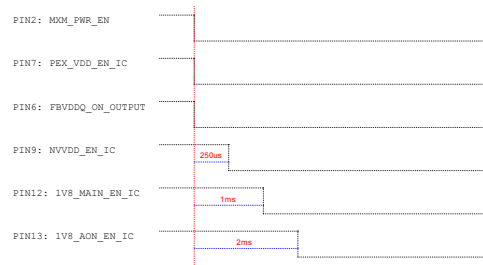


PIN2: MXM_PWR_EN is 3.3V INPUT
 PIN3: GPIO4_GC6_PWR_EN is 1.8V INPUT
 PIN4: FBVDDQ_ON_INPUT 3.3V INPUT
 PIN6: FBVDDQ_ON_OUTPUT 3.3V OUTPUT
 PIN7: PEX_VDD_EN IC 3.3V OUTPUT
 PIN9: NVVDD_EN IC 3.3V OUTPUT
 PIN12: 1V8_MAIN_EN IC 3.3V OUTPUT
 PIN13: 1V8_AON_EN_IC 3.3V OUTPUT

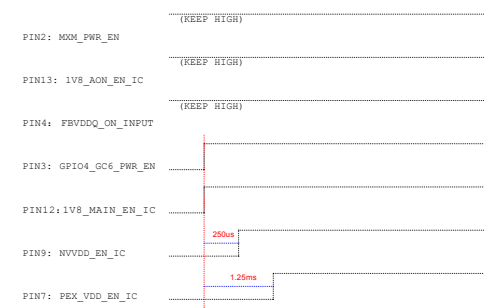
Power Up Sequence



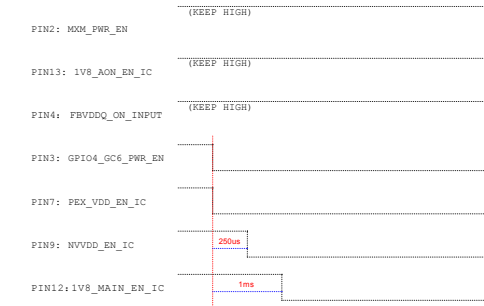
Power Down Sequence



GC6 2.1 Exit Sequence

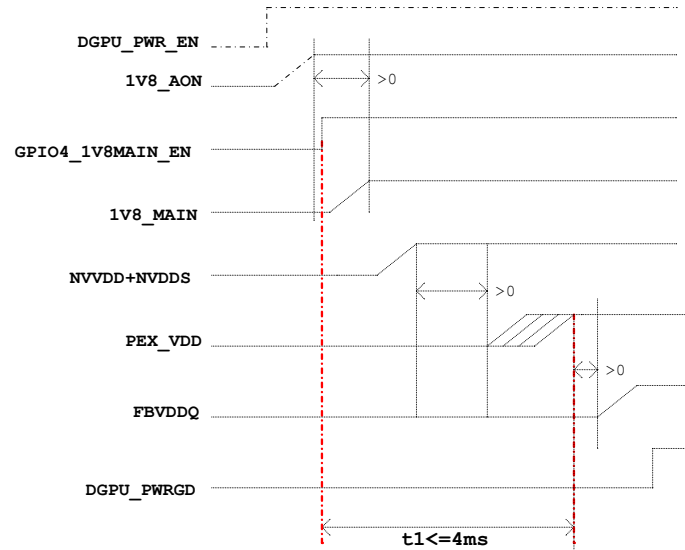


GC6 2.1 Entry Sequence



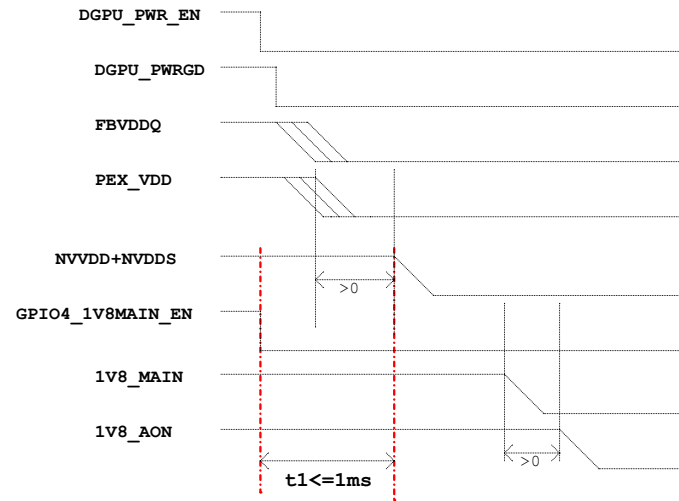
POWER UP Sequence

1V8_AON -> 1V8_MAIN->NV3V3 -> NVVDD -> NVVDDS / PEX_VDD -> FBVDDQ

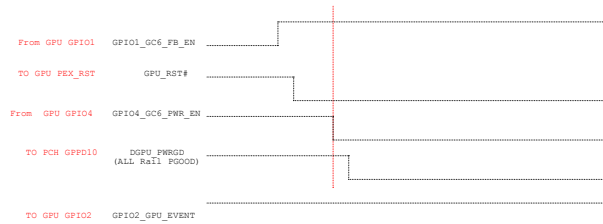


POWER Down Sequence

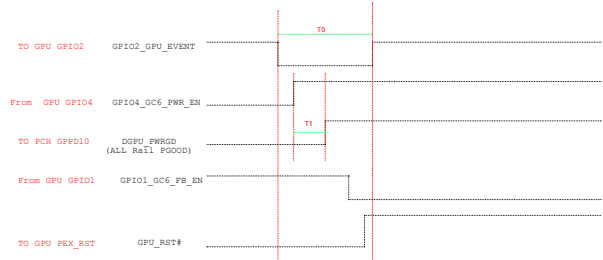
NVVDDS/PEX_VDD/FBVDDQ ->NVVDD/NV3V3->1V8_MAIN> 1V8_AON



GC6 2.1 ENTRY SEQUENCE



GC6 2.1 EXIT SEQUENCE



GC6 2.1 TIMING

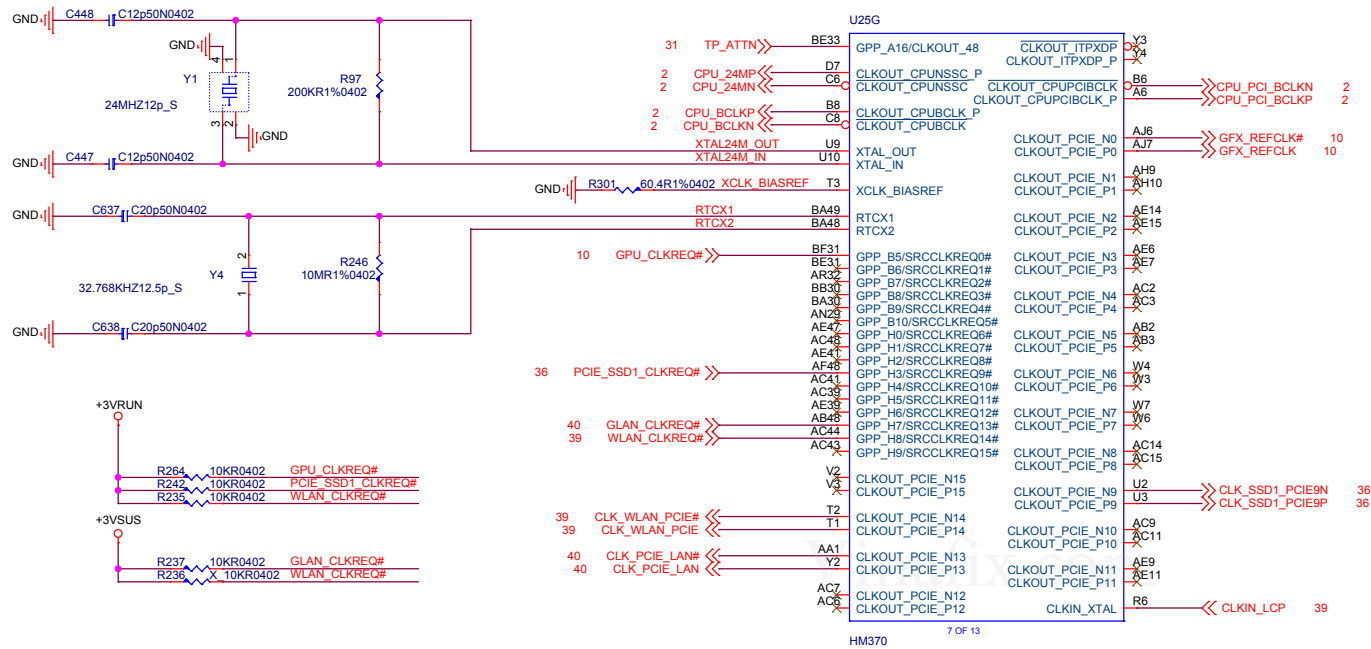
	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU EVENT# assertion
T1	0.04	4	ms	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

- ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry and exit sequence must complete within 200 ms.

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HM370 (RTC/PCIE_Clock/Clock/RSVD)



Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

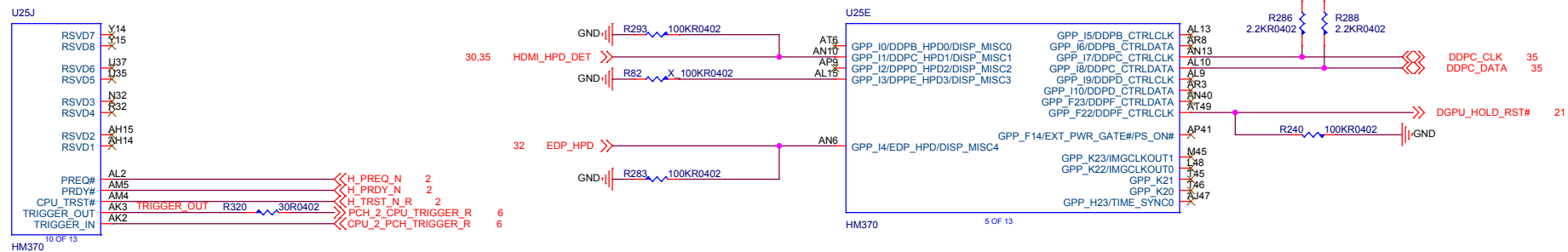
DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

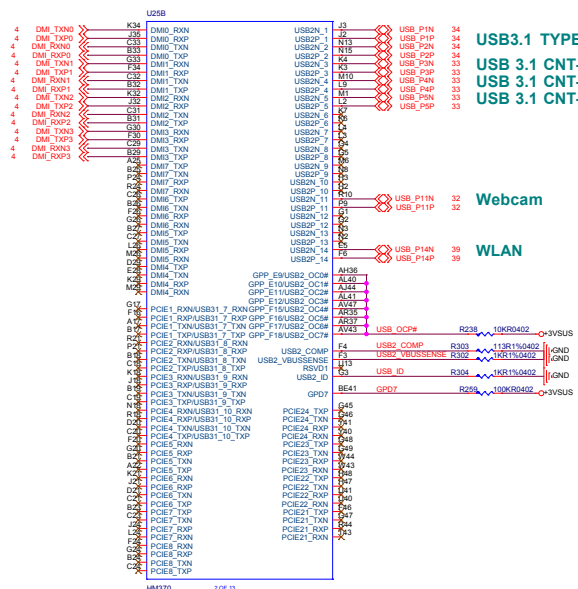
GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

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HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)

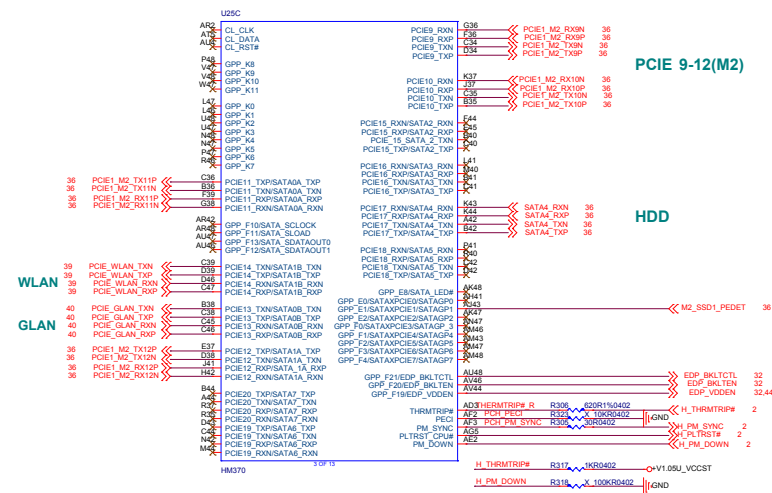


USB			
USB 2.0	USB 3.1	Device	Note
1	1	USB TYPE_C-1	
2	3	USB TYPE_C-2	
3	3	USB TYPE_A-1	
4	4	USB TYPE_A-2	
5	5	USB TYPE_A-3	
6			
7			
8			
9			
10			
11		WebCam	
12			
13			
14		WLAN	

GPD7
External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

High Speed I/O Ports				
	FM370		Device	
1	USB3.1 Gen 1		NC	
2	USB3.1 Gen 1		NC	
3	N/A		NC	
4	N/A		NC	
5	INTEL LAN Only		NC	
6	N/A		NC	
7	N/A		NC	
8	N/A		NC	
9	PCIe/LAN	PICE Configurable M.2	M.2 SSD-1	
10	PCIe			
11	PCIe/SATA0A			
12	PCIe/LAN/SATA1A			
13	PCIe/LAN/SATA0B			LAN
14	PCIe/SATA1B			WLAN
15	PCIe			NC
16	PCIe			NC
17	PCIe/SATA4		HDD	
18	PCIe/SATA5		NC	
19	PCIe		NC	
20	PCIe		NC	
21	PCIe		NC	
22	PCIe			
23	PCIe			
24	PCIe			

SATA Lane 0 has the flexibility to be mapped to PCIE 11 or 13
SATA Lane 1 has the flexibility to be mapped to PCIE 12 or 14



GPP J4 / CNV BRI DT

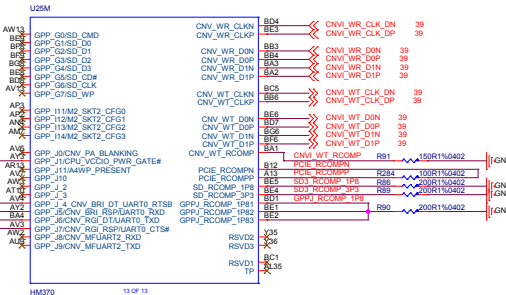
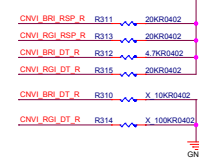
This signal has a weak internal pull-down. An external pull-up is required on this strap. MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

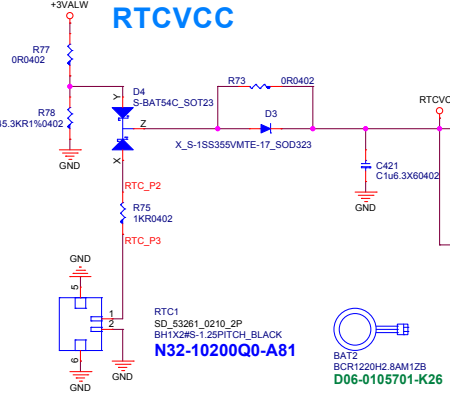
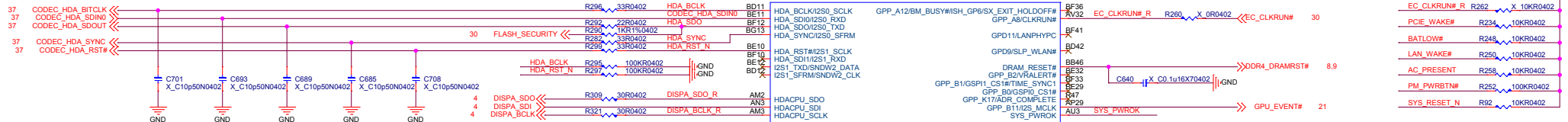
GPP J6 / CNV RGI DT

An external pull-up or pull-down is required
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

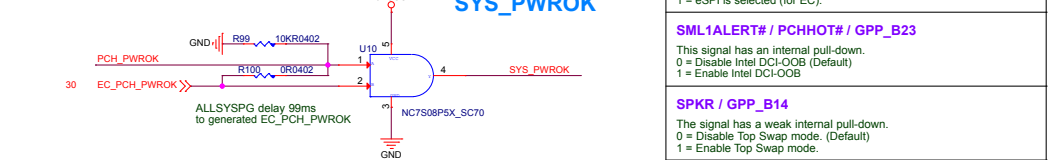
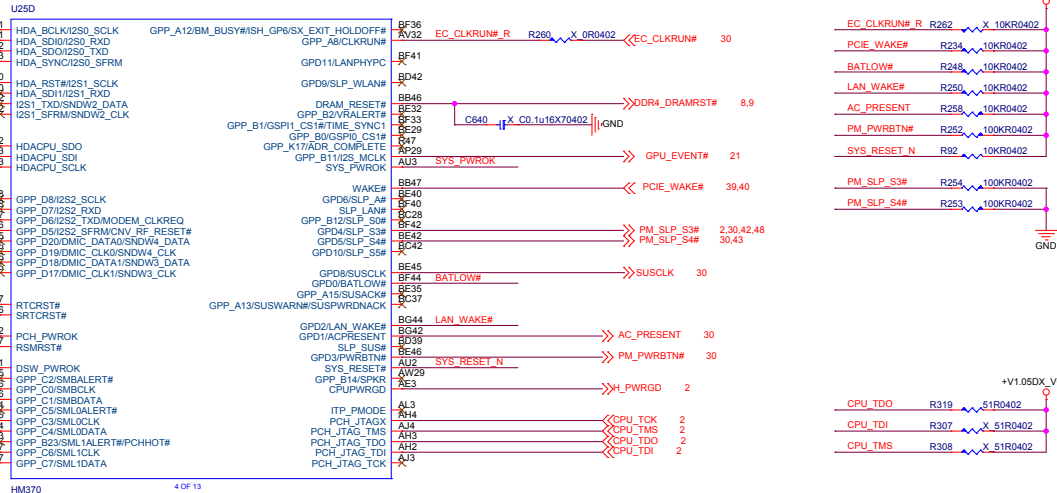
GPP J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail





A B C D E

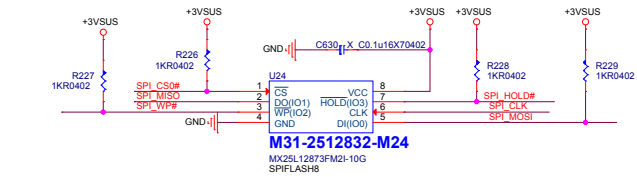


A B C D E

Functional Strap Definitions	
HDA_SDO / I2S0_TXD	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override).
SMBALERT# / GPP_C2	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected (for EC). (Default) 1 = eSPI is selected (for EC).
SML1ALERT# / PCHHOT# / GPP_B23	This signal has an internal pull-down. 0 = Disable Intel DCI-OOB (Default) 1 = Enable Intel DCI-OOB
SPKR / GPP_B14	The signal has a weak internal pull-down. 0 = Disable Top Swap mode. (Default) 1 = Enable Top Swap mode.
DG/ RTC Well Input Strap	
RSMRST# & DSW_PWROK, PCH_PWROK : PD RTCST# & SRTCST# & INTRUDER# : PU	

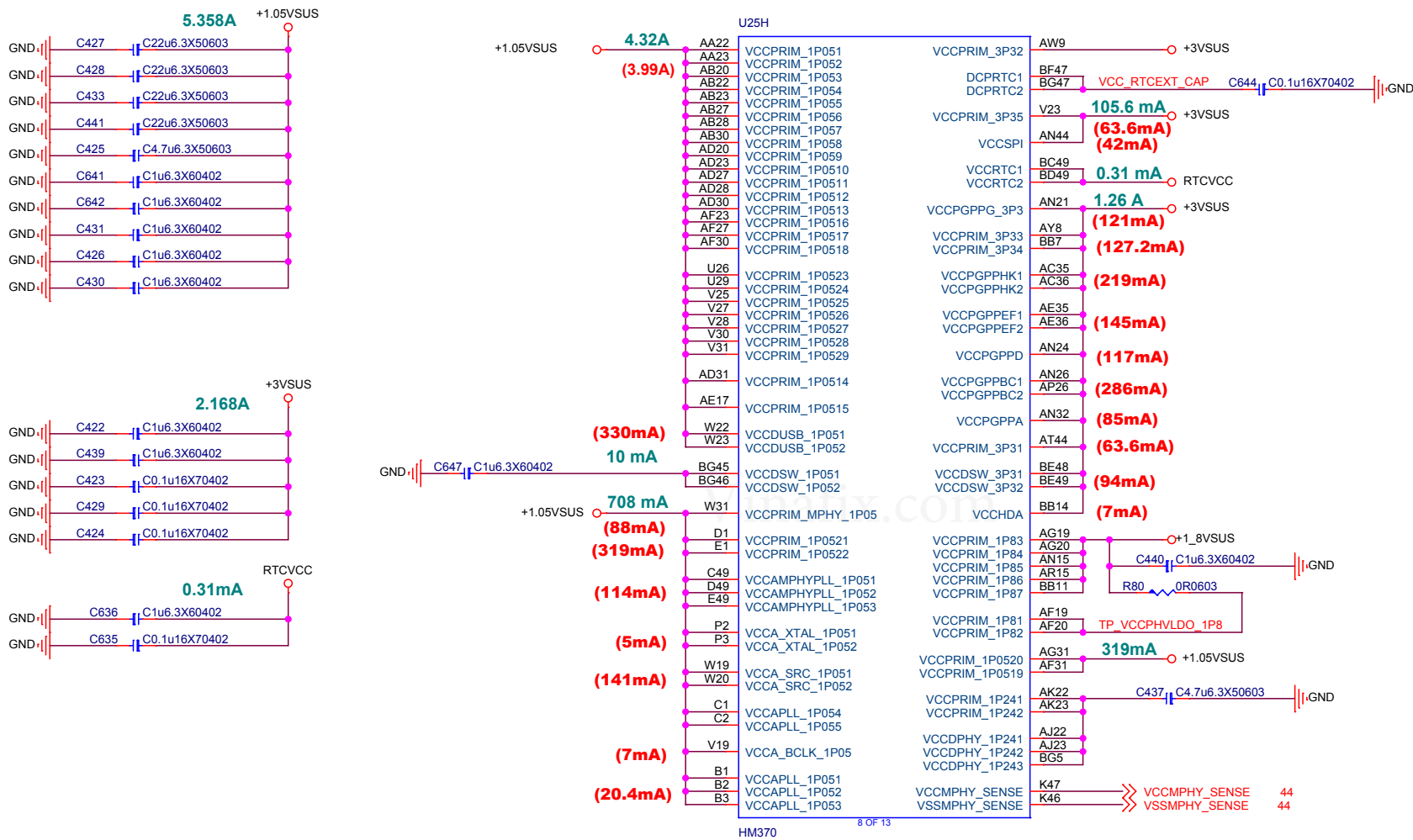
msi MICRO-STAR INT'L CO.,LTD.	
Title	PCH-3(HDA/RTC/SMBUS)
Size	Document Number
Customer	MS-16R1
Date	Wednesday, April 11, 2018
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Rev	1.0

SPI FLASH ROM 16MB

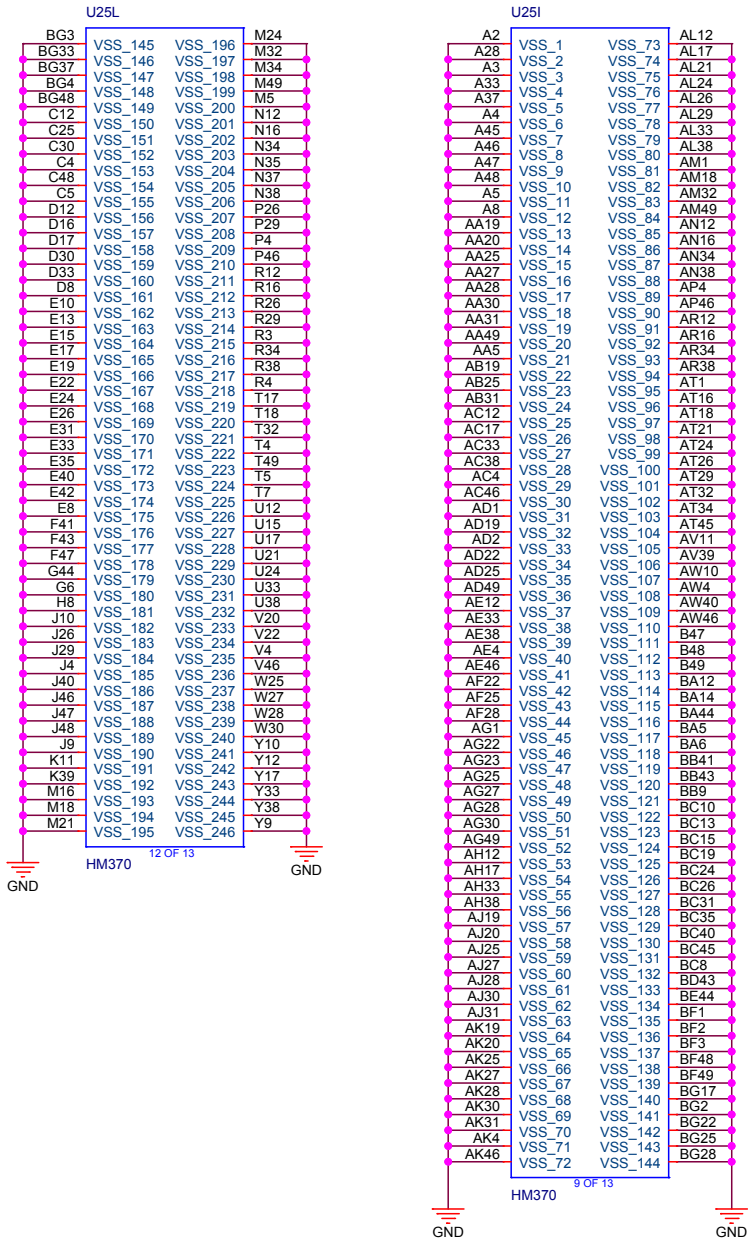
[illegible]

GSPI0_MOSI / GPP_B18
The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

HM370 (Power)



PCH-H(GND)



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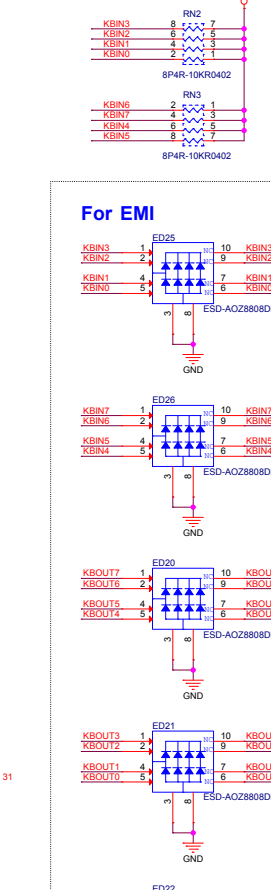
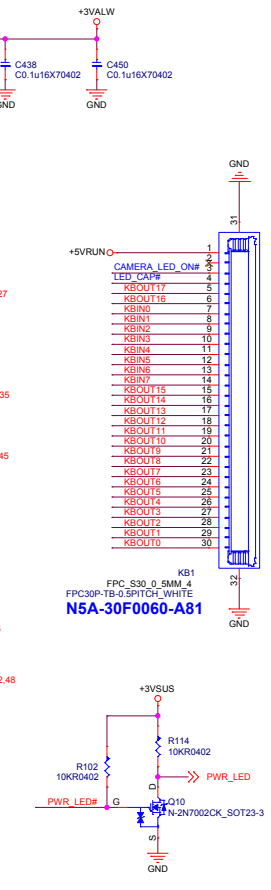
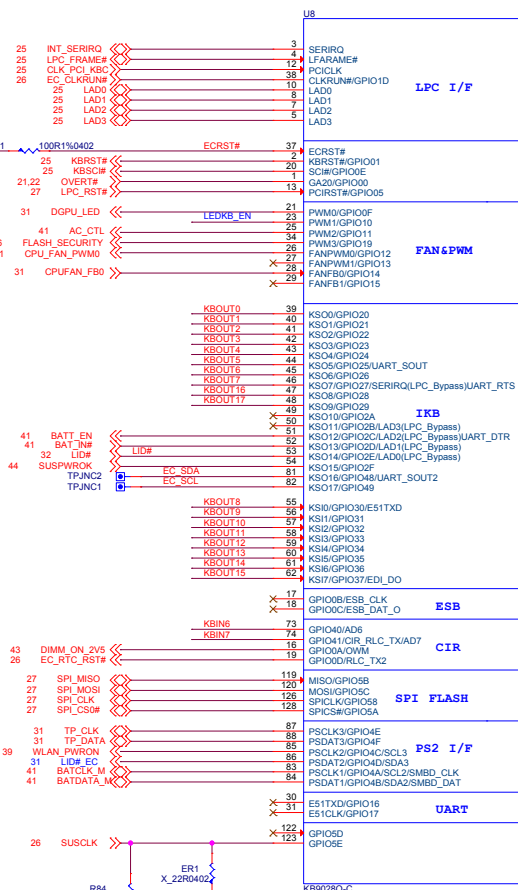
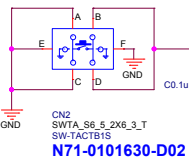


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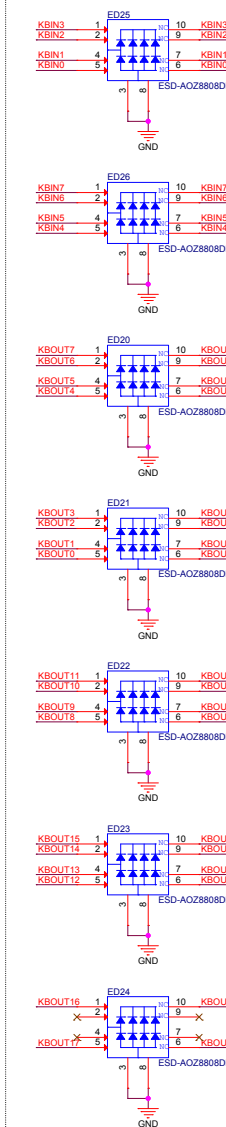
Title		PCH-6(GND)	
Size	Document Number	Rev	1.0
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KBC/EC/uP (ENE9028)

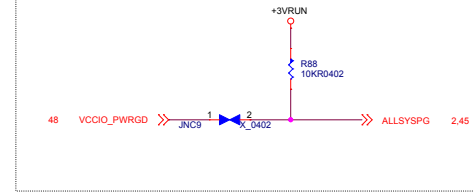
Hardware Reset



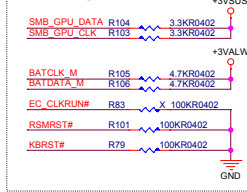
For EMI



ALLSYSPPG



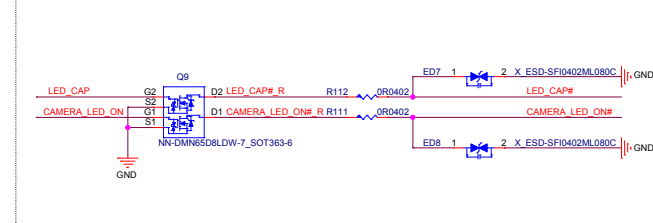
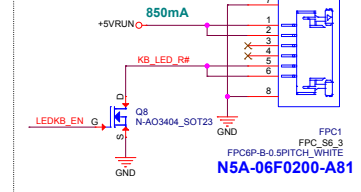
Pull Up/Pull Down



MB_ID

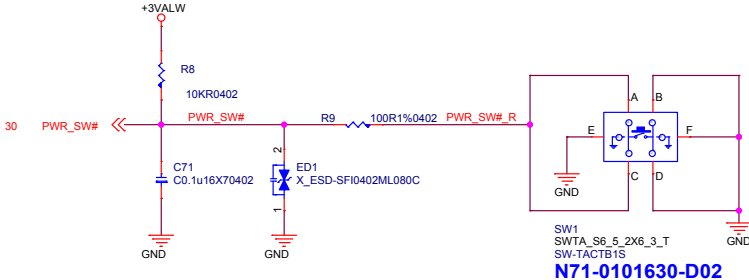


Keyboard LED CONN

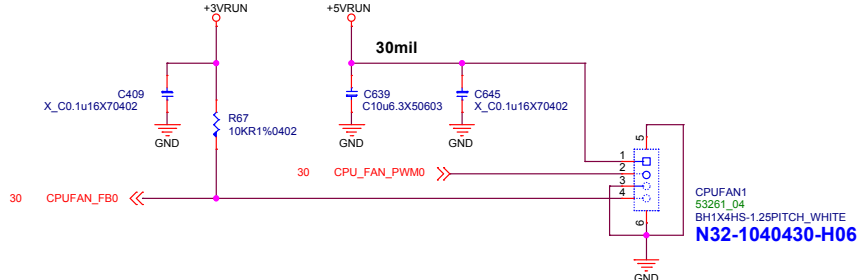


Power Switch / FAN / Touch Pad / LED

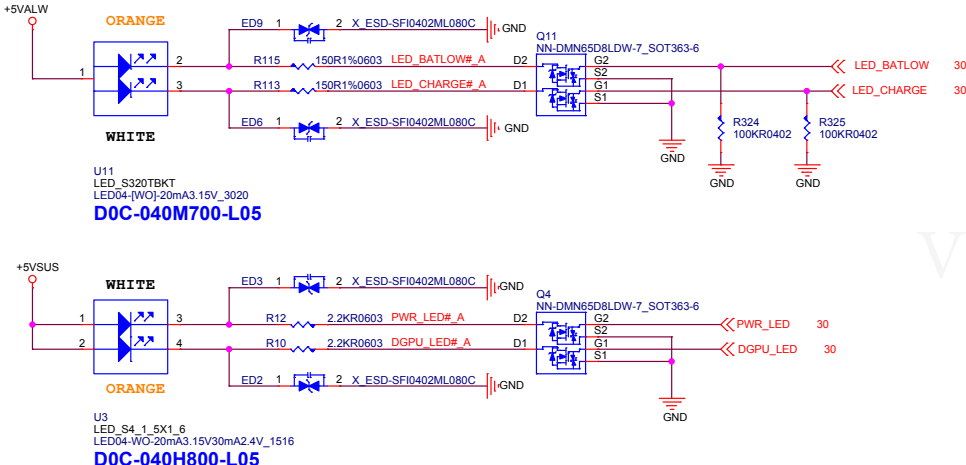
Power Switch



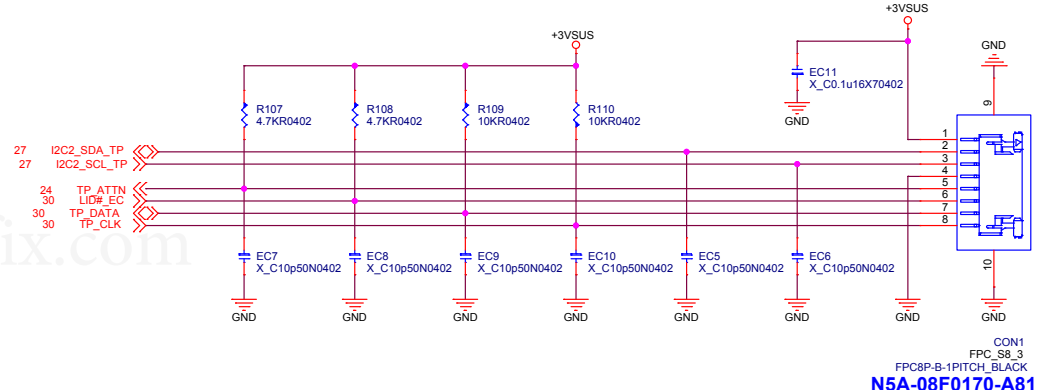
CPU FAN



LED

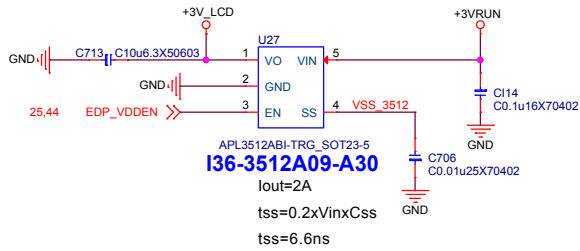


Touch Pad Board

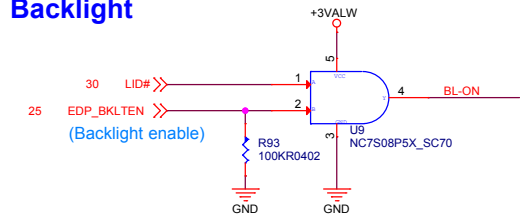


 MICRO-STAR INT'L CO.,LTD.	
Title Power Switch/FAN/Touch Pad/LED	
Size Custom	Document Number MS-16R1
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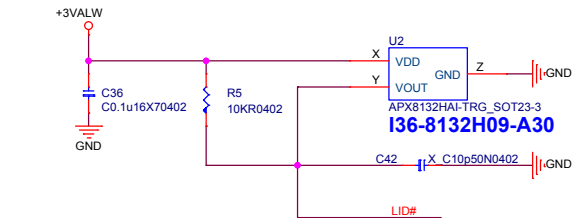
Pannel Device Logic Power



Backlight



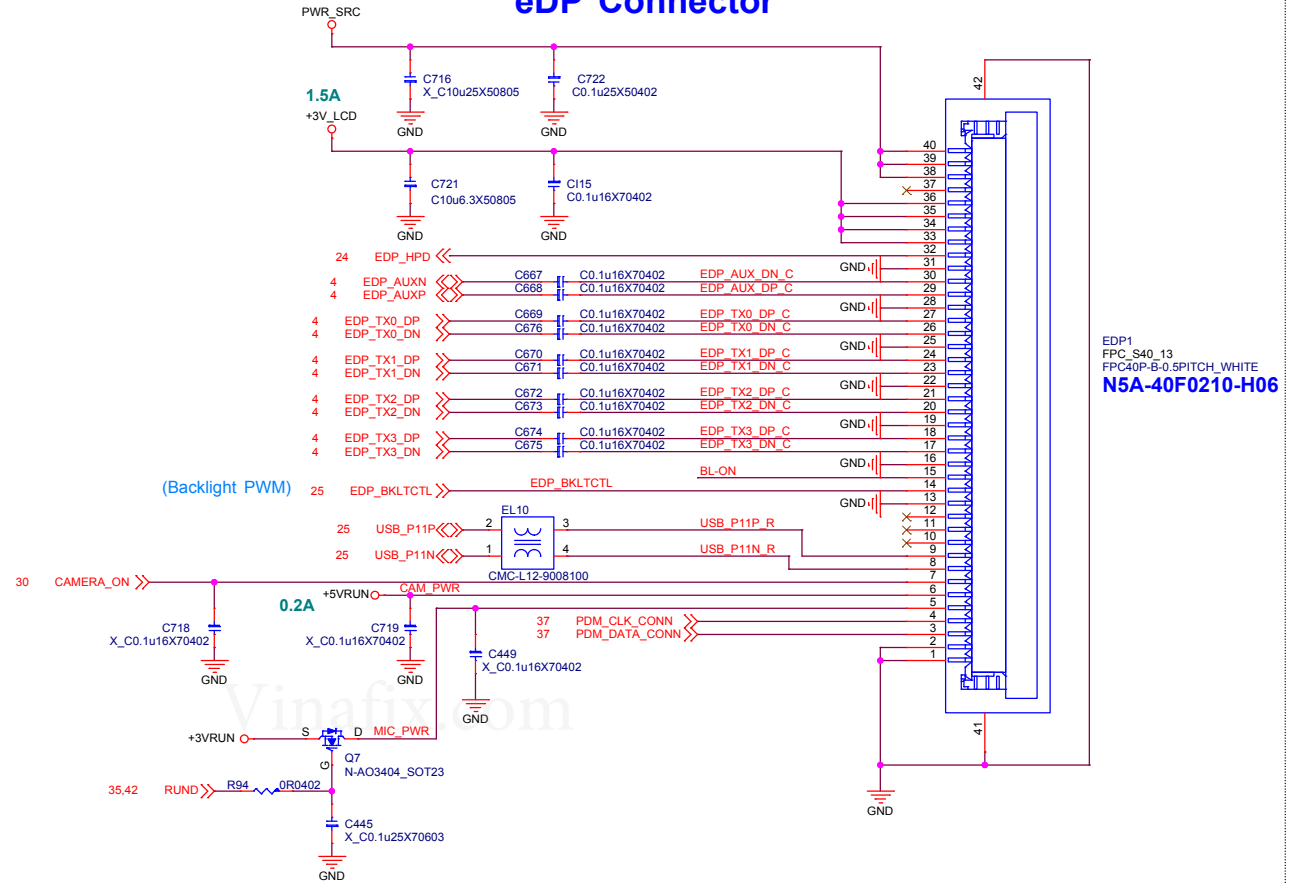
Hall Switch



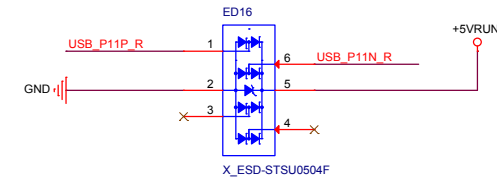
EMI Close Connector



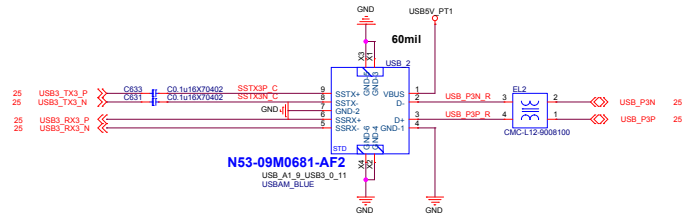
eDP Connector



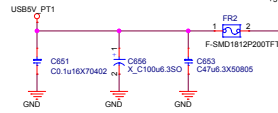
ESD



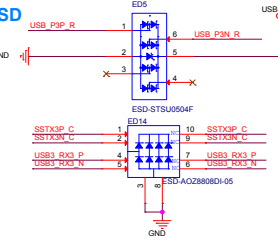
USB3.0 CNT-1



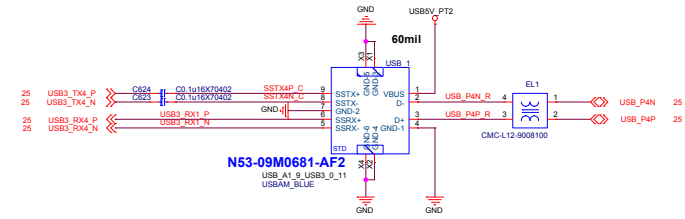
USB Power Switch



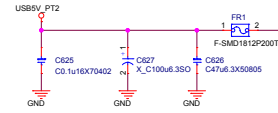
ESD



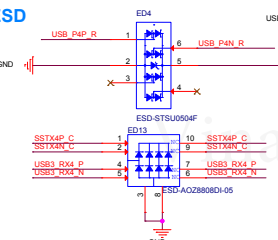
USB3.0 CNT-2



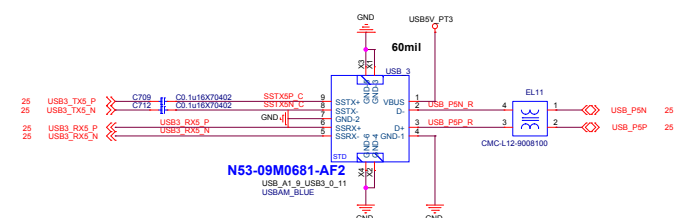
USB Power Switch



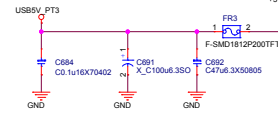
ESD



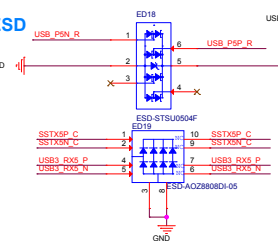
USB3.0 CNT-3



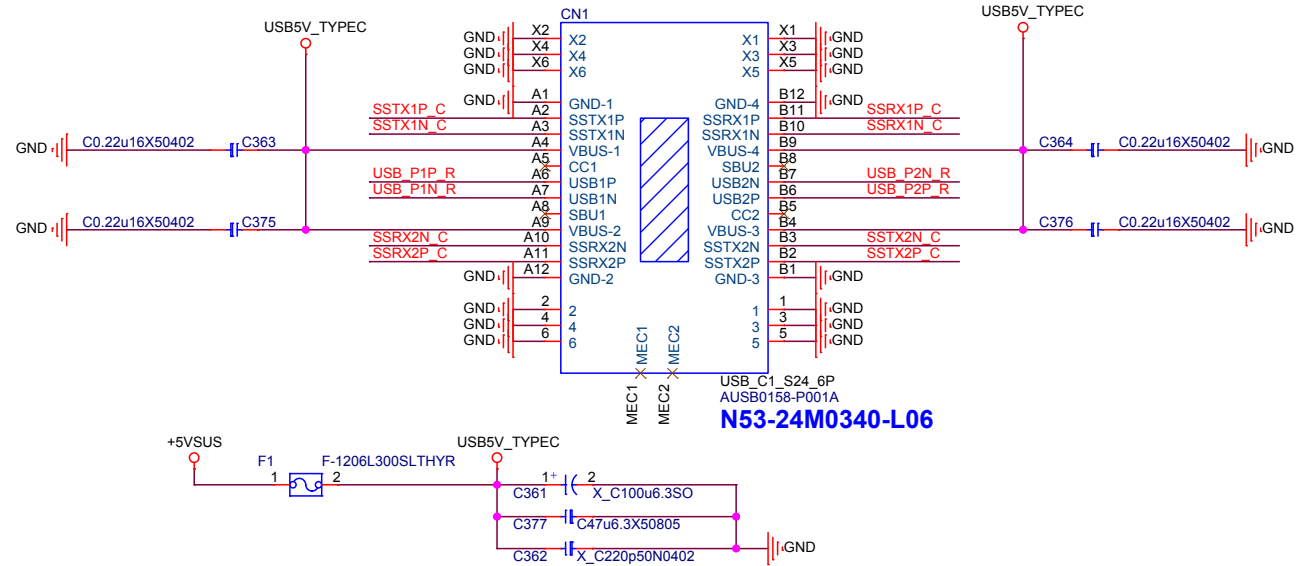
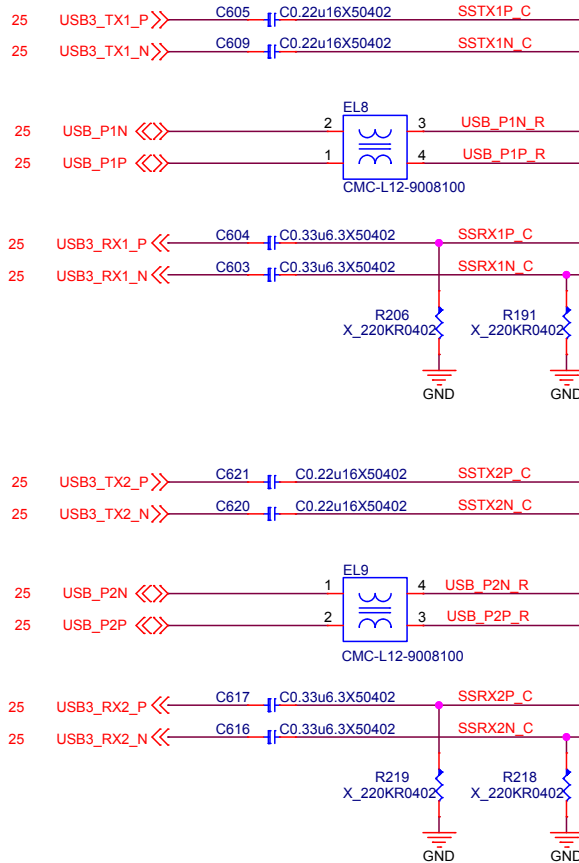
USB Power Switch



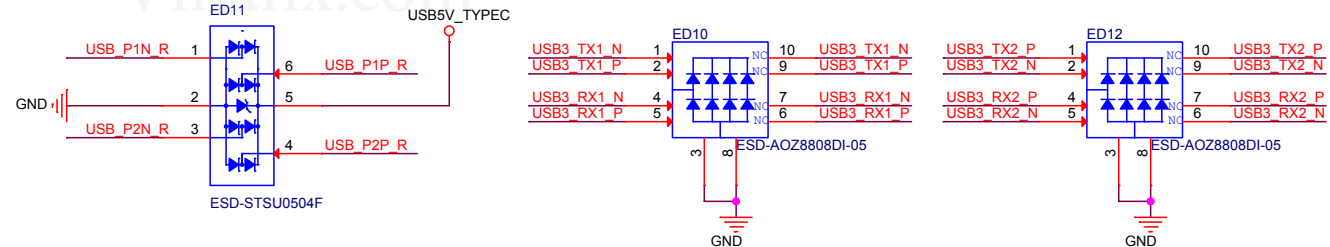
ESD



USB 3.0 TYPE_C



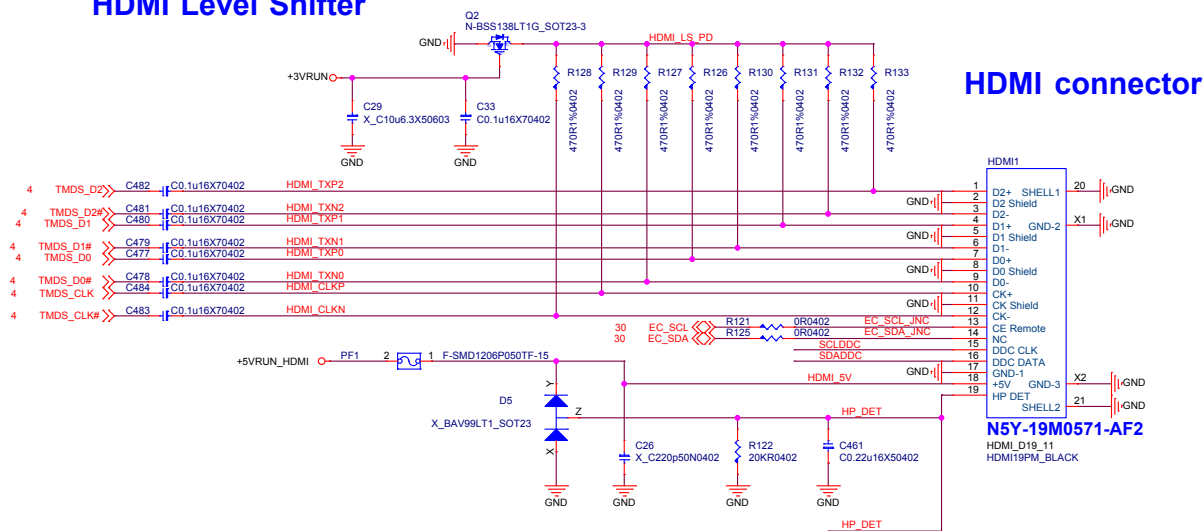
ESD



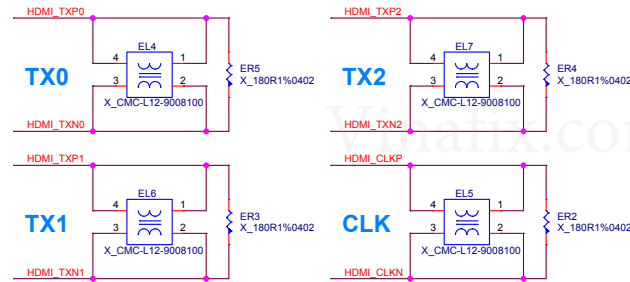
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Title			
USB 3.0 TYPE_C			
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HDMI Level Shifter

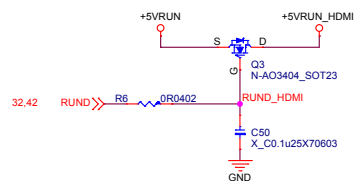


EMI Close Connector

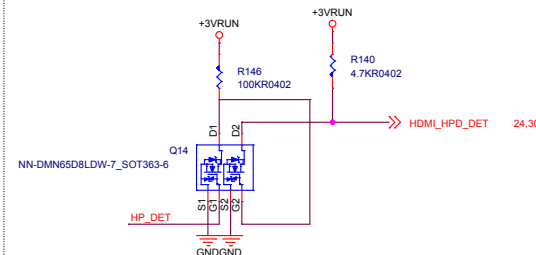


Avoid HDMI Leakage

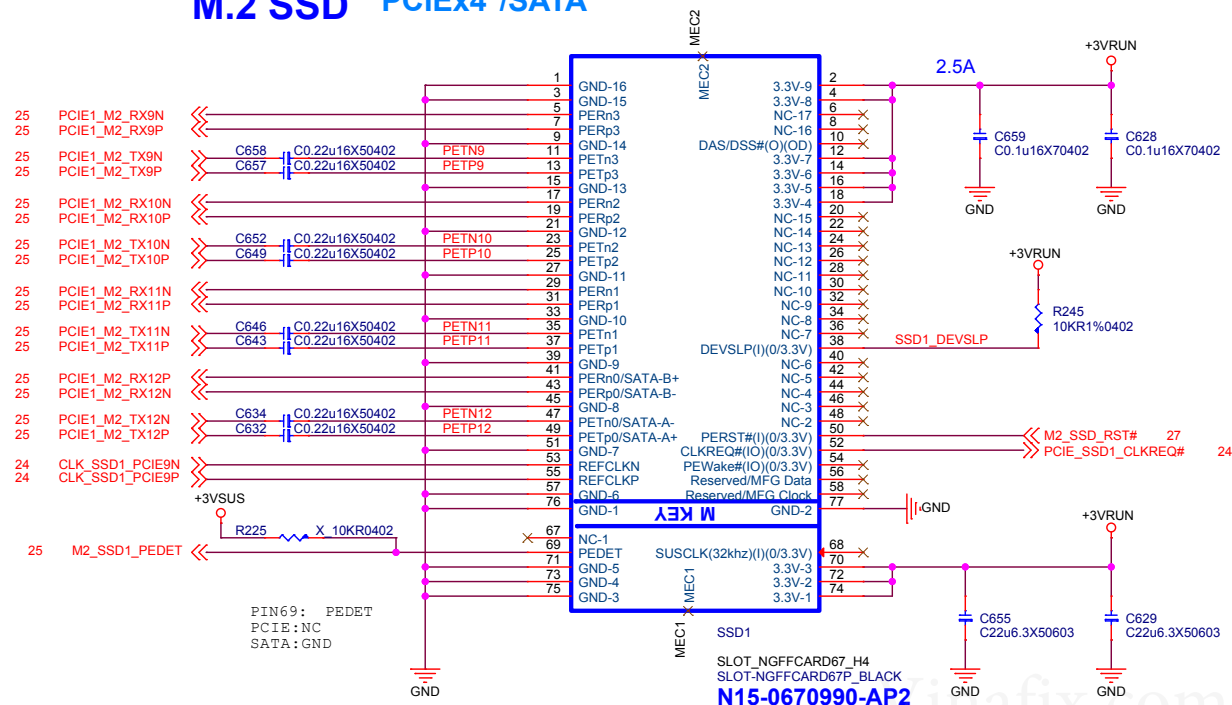
W>20mils



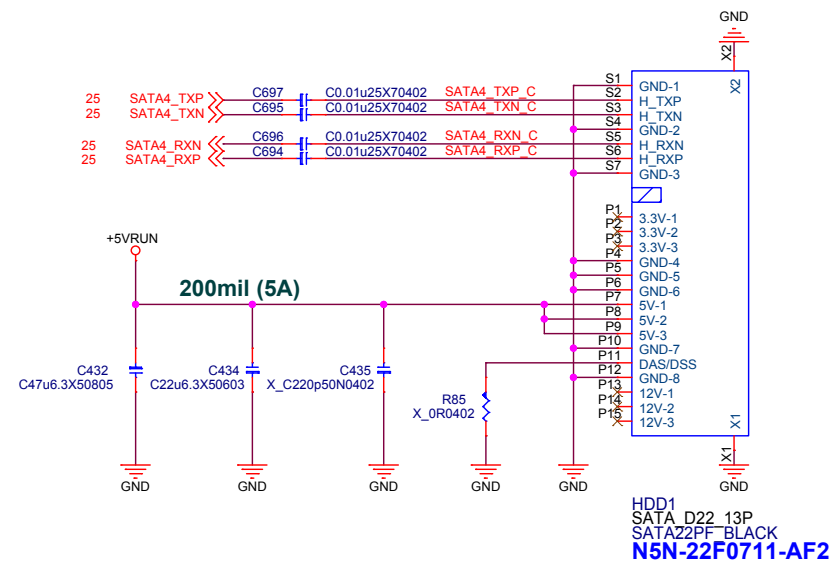
HPD Level Shift 5V to 3V for Debug Card



M.2 SSD PCIe4 /SATA



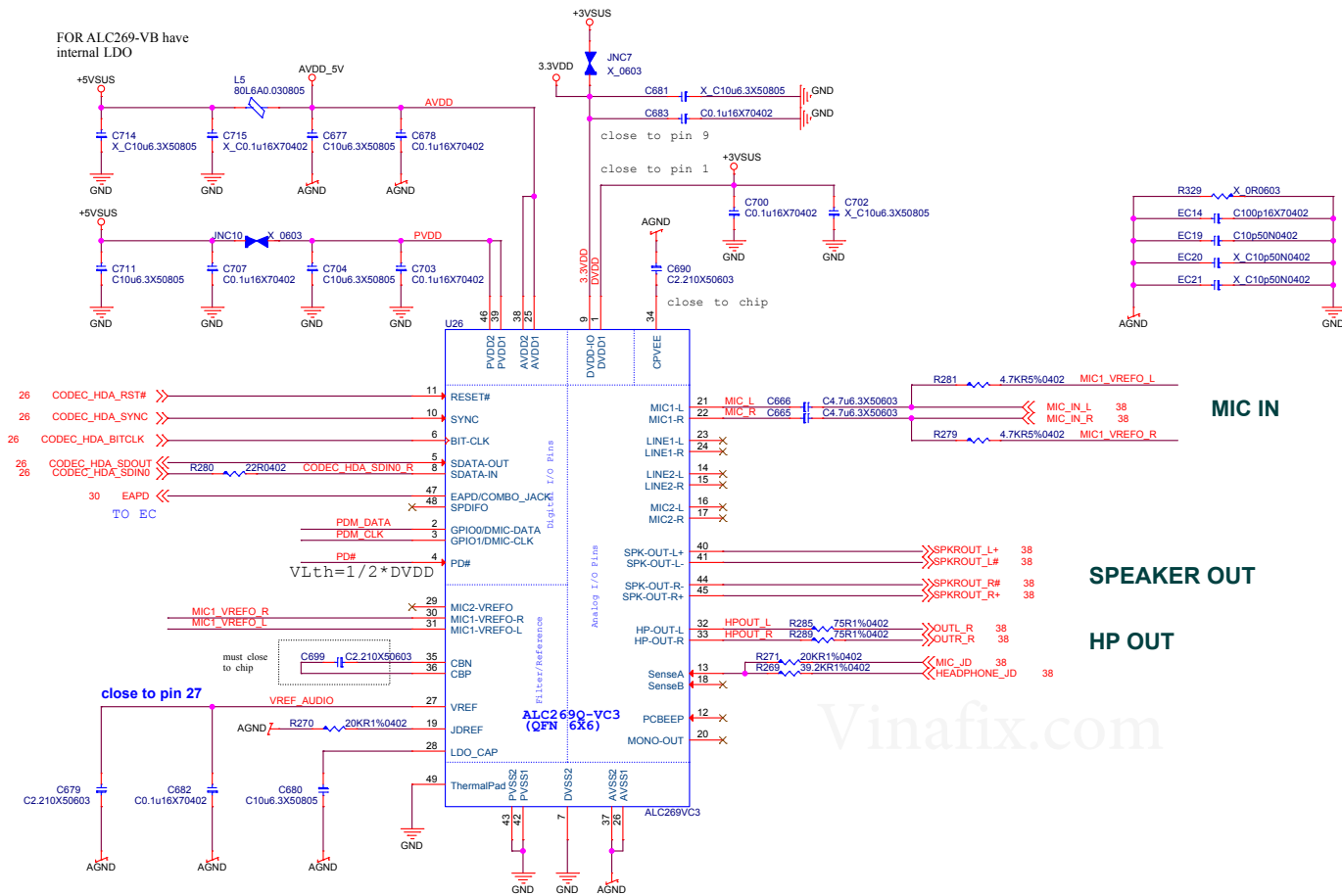
HDD



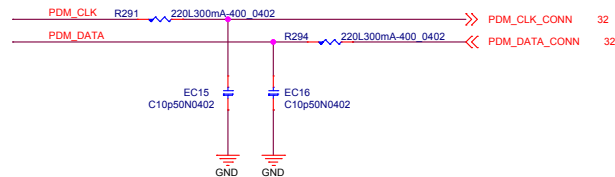
msi MICRO-STAR INT'L CO.,LTD.

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M.2 SSD/HDD		
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FOR ALC269-VB have
internal LDO

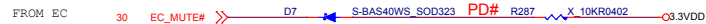


EMI Close Codec



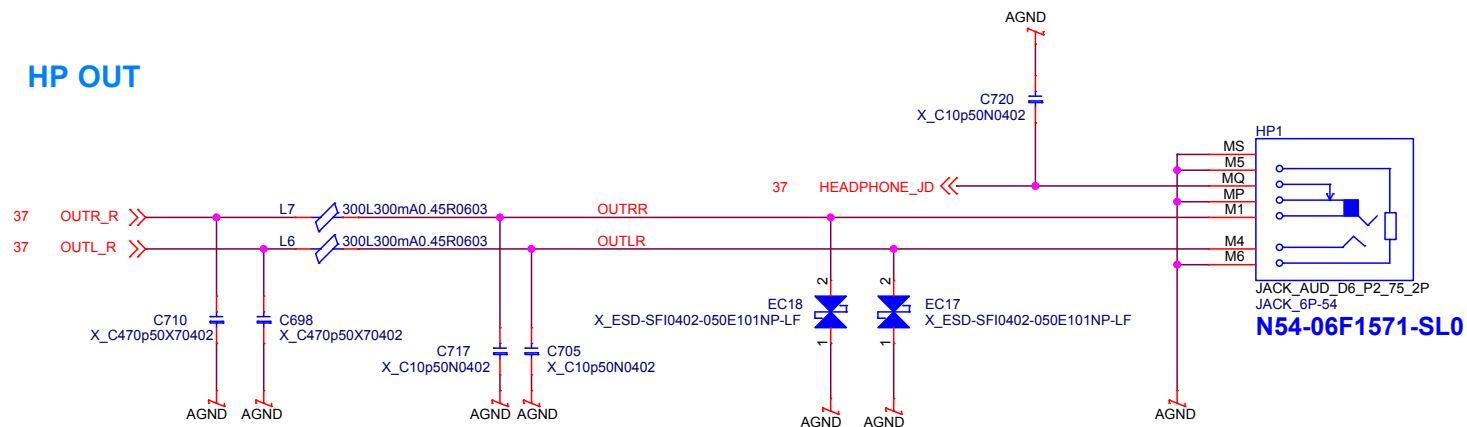
Internal Mic

simple MUTE

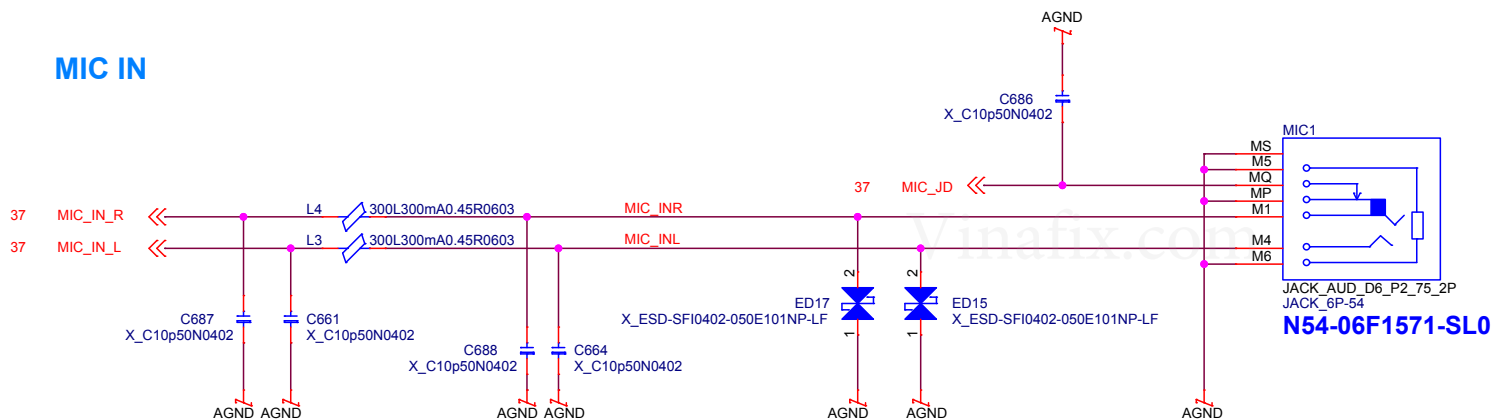


Audio CONN

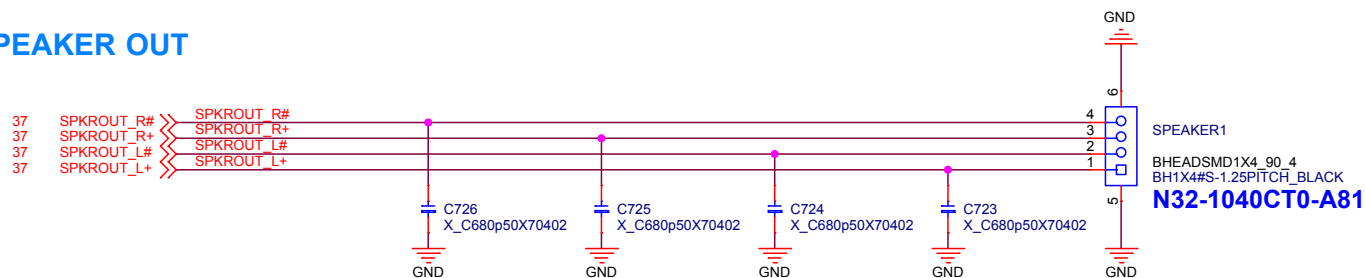
HP OUT



MIC IN



SPEAKER OUT

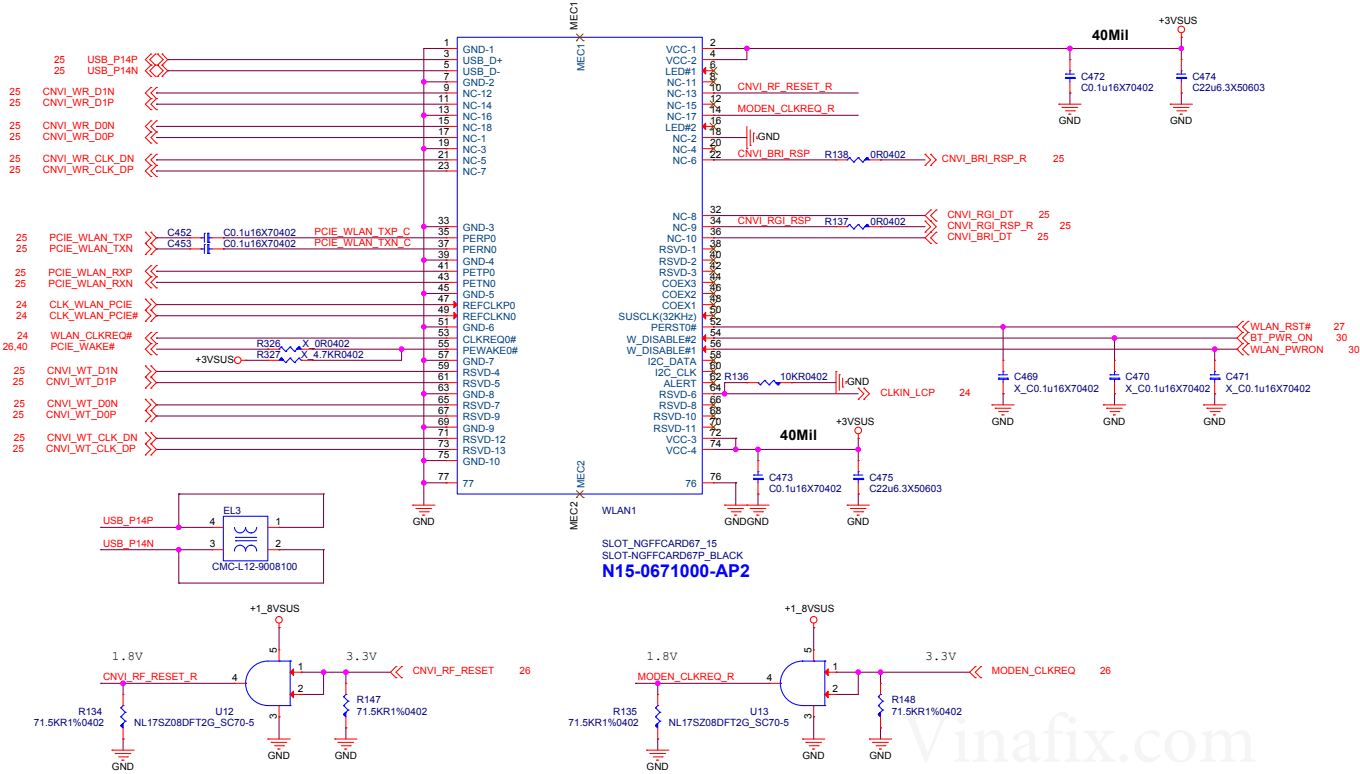


msi

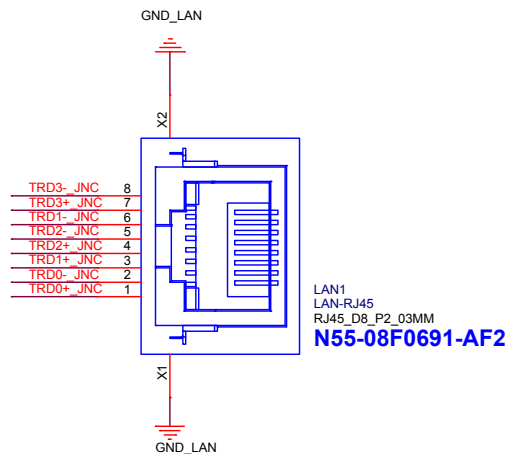
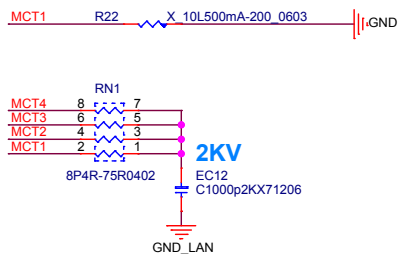
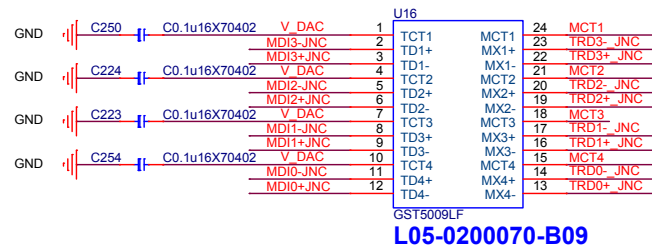
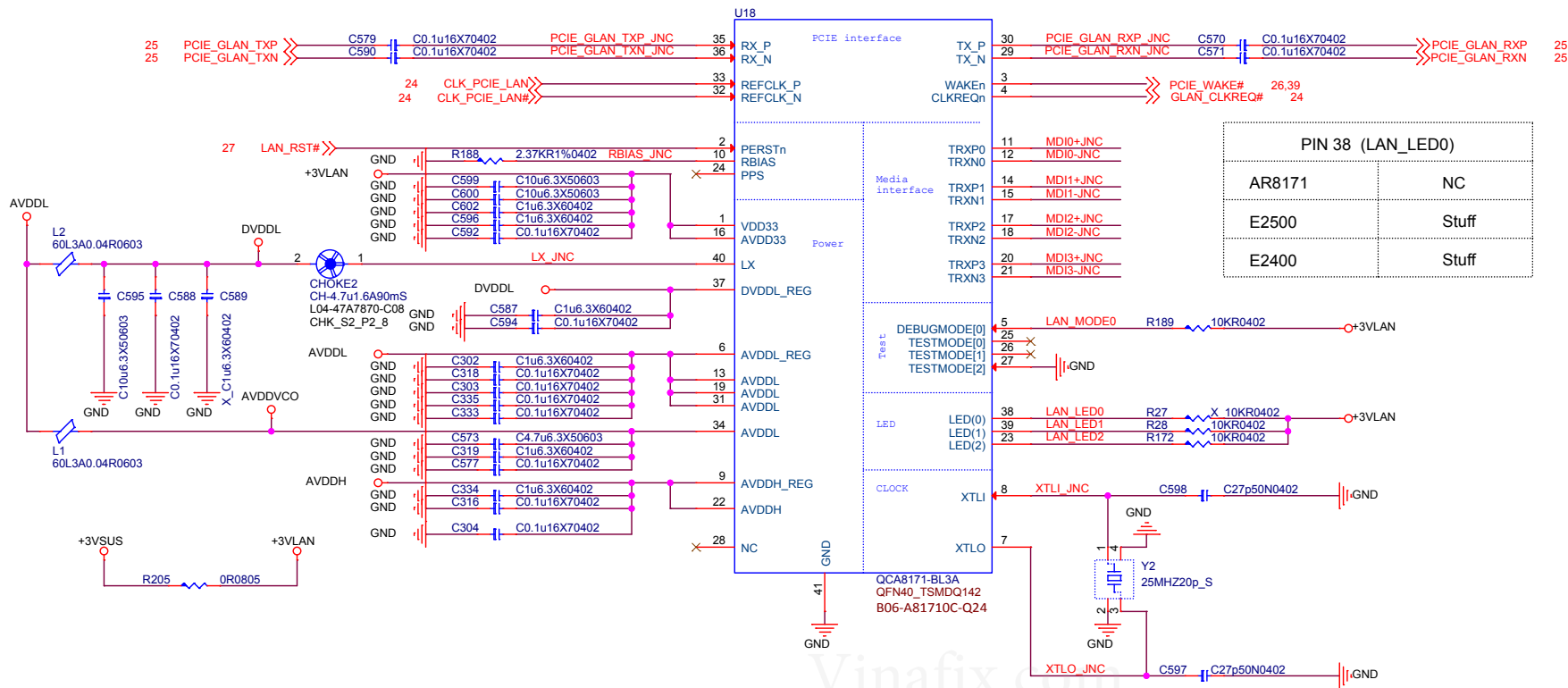
MICRO-STAR INT'L CO.,LTD.

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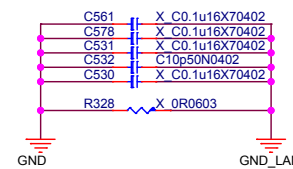
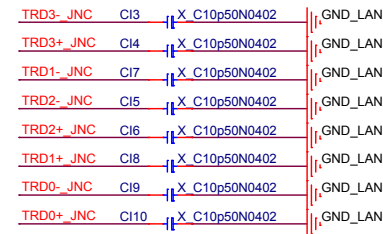
WLAN



Pin #	M.2 WLAN	Intel CNVI WLAN	Pin #	M.2 WLAN	Intel CNVI WLAN
Pin 1	GND	GND	Pin 2	3.3V	3.3V
Pin 3	USB_D+	N/C	Pin 4	3.3V	3.3V
Pin 5	USB_D-	N/C	Pin 6	LED1#	LED1#
Pin 7	GND	GND	Pin 8	Module Key	N/C
Pin 9	Module Key	WGR_D1N	Pin 10	Module Key	RF_RESET_B(1.8V)
Pin 11	Module Key	WGR_D1P	Pin 12	Module Key	N/C
Pin 13	Module Key	GND	Pin 14	Module Key	CLKREQ0(1.8V)
Pin 15	Module Key	WGR_D0N	Pin 16	LED2#	LED2#
Pin 17	N/C	WGR_D0P	Pin 18	GND	GND
Pin 19	N/C	GND	Pin 20	N/C	N/C
Pin 21	N/C	WGR_CLKN	Pin 22	N/C	BRI_RSP(1.8V)
Pin 23	N/C	WGR_CLKP	Pin 24	Module Key	Module Key
Pin 25	Module Key	Module Key	Pin 26	Module Key	Module Key
Pin 27	Module Key	Module Key	Pin 28	Module Key	Module Key
Pin 29	Module Key	Module Key	Pin 30	Module Key	Module Key
Pin 31	Module Key	Module Key	Pin 32	N/C	RGI_DT(1.8V)
Pin 33	GND	GND	Pin 34	N/C	RGI_RSP(1.8V)
Pin 35	PERP0	N/C	Pin 36	N/C	BGI_DT(1.8V)
Pin 37	PERN0	N/C	Pin 38	N/C	N/C
Pin 39	GND	GND	Pin 40	N/C	N/C
Pin 41	PETP0	N/C	Pin 42	N/C	N/C
Pin 43	PETN0	N/C	Pin 44	N/C	N/C
Pin 45	GND	GND	Pin 46	N/C	N/C
Pin 47	REFCLKP0	N/C	Pin 48	N/C	N/C
Pin 49	REFCLKN0	N/C	Pin 50	SUSCLK (32KHz)	SUSCLK (32KHz)
Pin 51	GND	GND	Pin 52	PERST0#	N/C
Pin 53	CLKREQ0#	N/C	Pin 54	BT_EN (W_DISABLE2#)	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	N/C	Pin 56	WLAN_EN (W_DISABLE2#)	WLAN_EN (W_DISABLE2#)
Pin 57	GND	GND	Pin 58	N/C	N/C
Pin 59	N/C	WT_D1N	Pin 60	N/C	N/C
Pin 61	N/C	WT_D1P	Pin 62	N/C	N/C
Pin 63	GND	GND	Pin 64	Resever	REFCLK0(38.4MKz)
Pin 65	N/C	WT_D0N	Pin 66	N/C	N/C
Pin 67	N/C	WT_D0P	Pin 68	N/C	N/C
Pin 69	GND	GND	Pin 70	N/C	N/C
Pin 71	N/C	WT_CLKN	Pin 72	3.3V	3.3V
Pin 73	N/C	WT_CLKP	Pin 74	3.3V	3.3V
Pin 75	GND	GND			

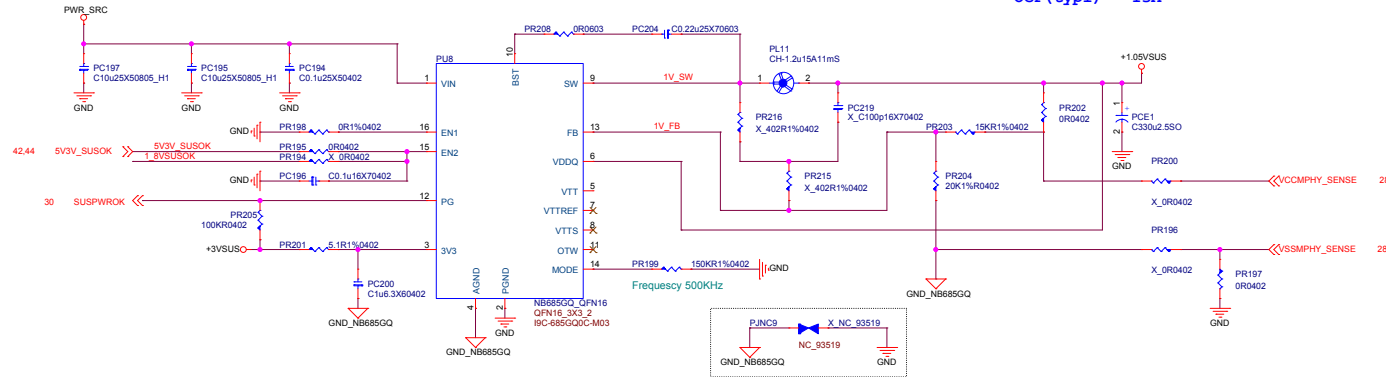


EMI



+1.05VSUS

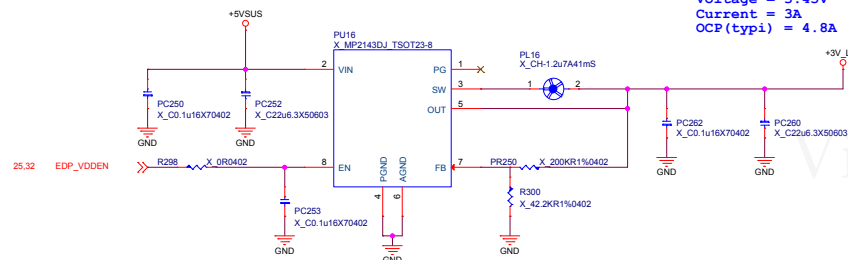
Voltage = 1.05V
Current = 10A
OCP(typi) = 13A



+3V_LCD

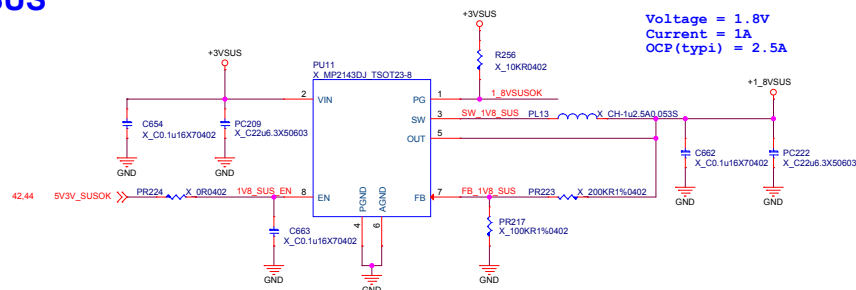
Pannel Device Logic Power

Voltage = 3.45V
Current = 3A
OCP(typi) = 4.8A

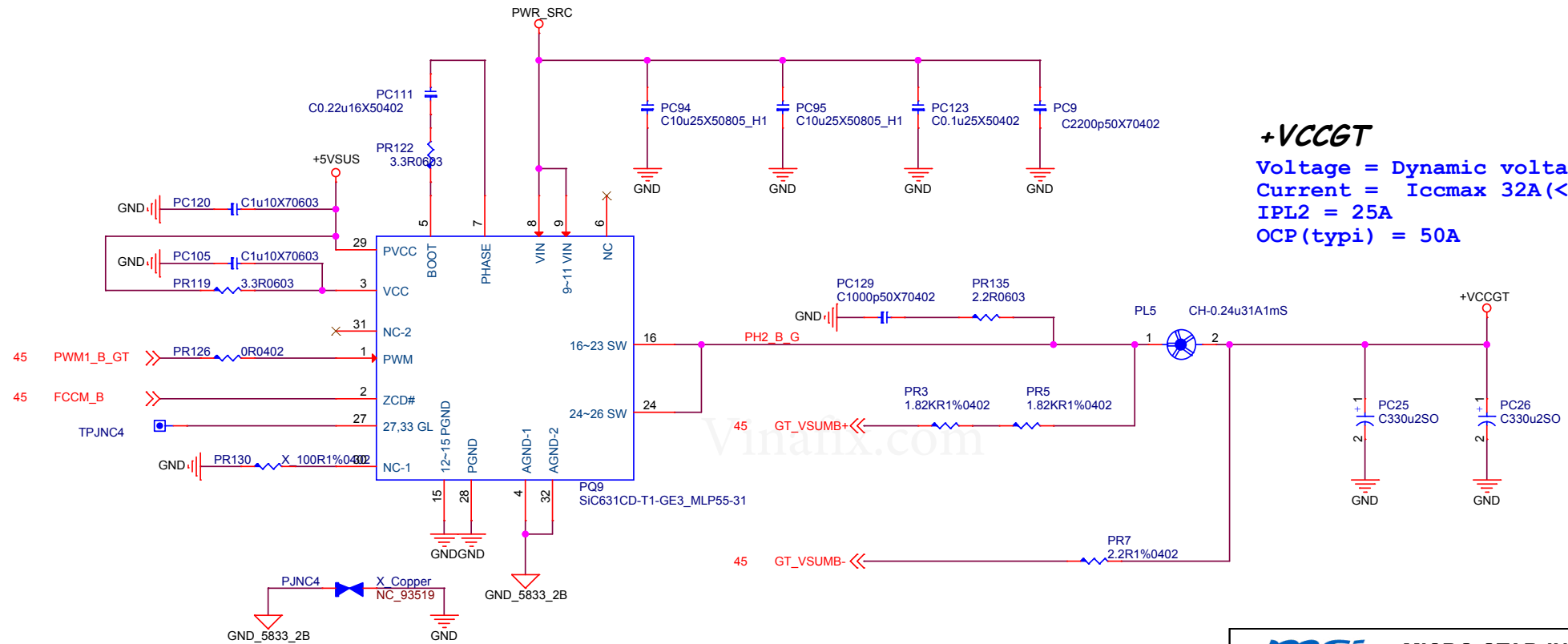


+1_8VSUS

Voltage = 1.8V
Current = 1A
OCP(typi) = 2.5A

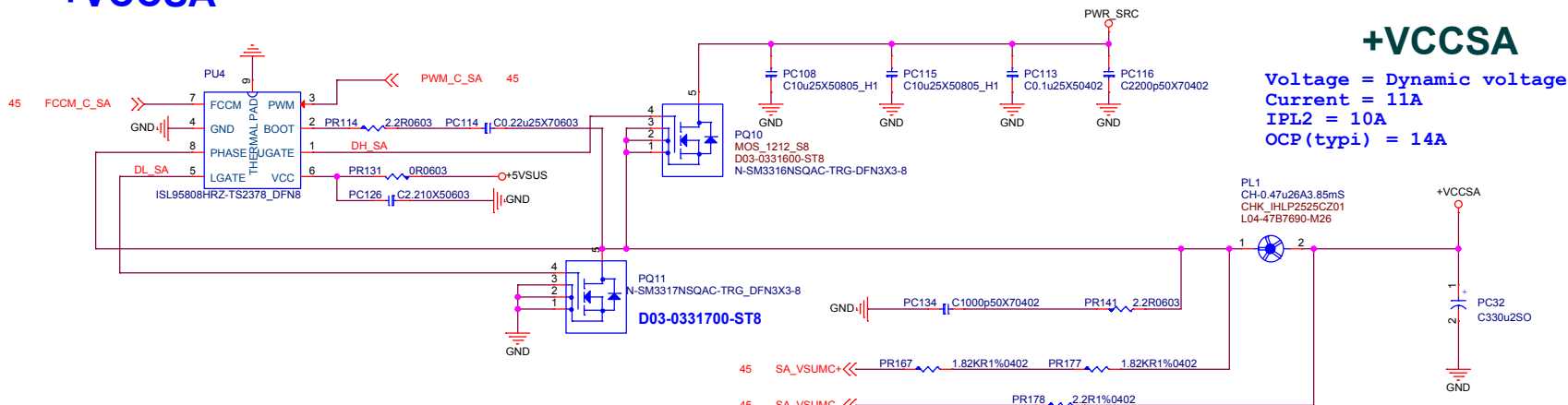


+VCCGT

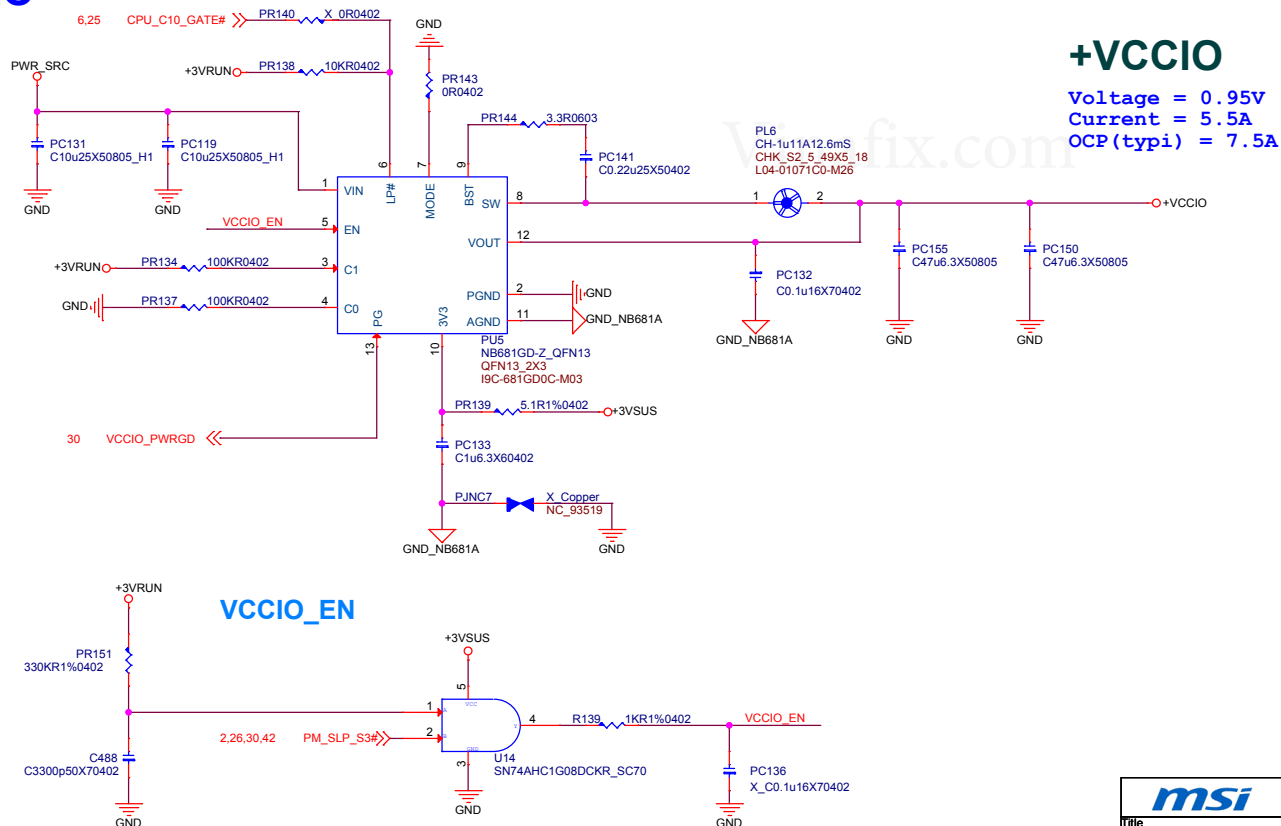


		MICRO-STAR INT'L CO.,LTD.	
Title			
CPU Power (VCCGT)			
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+VCCSA



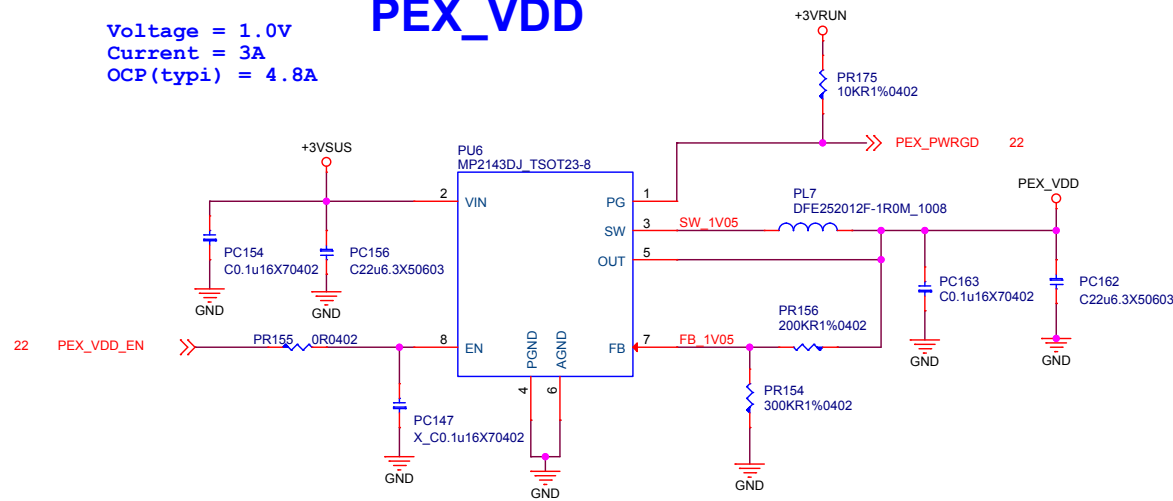
+VCCIO



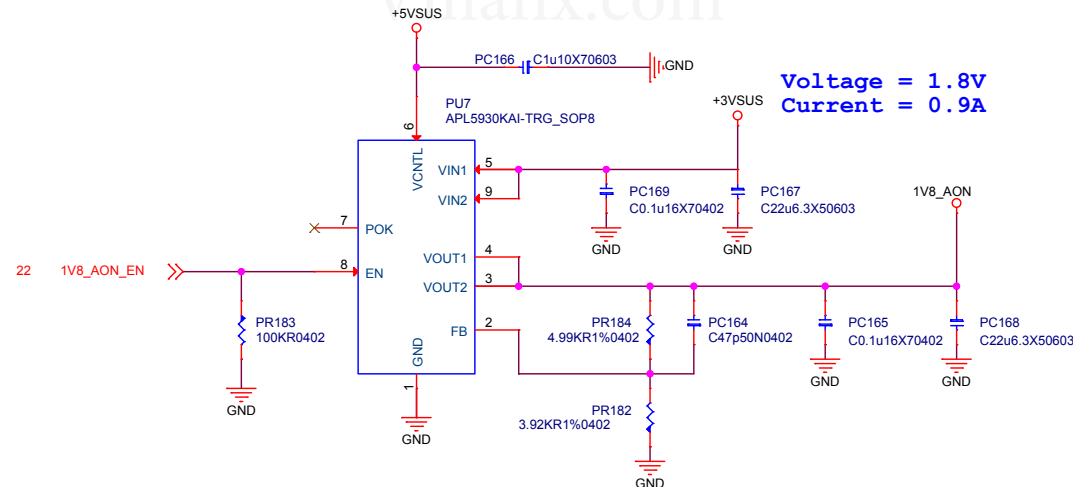
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Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A

PEX_VDD

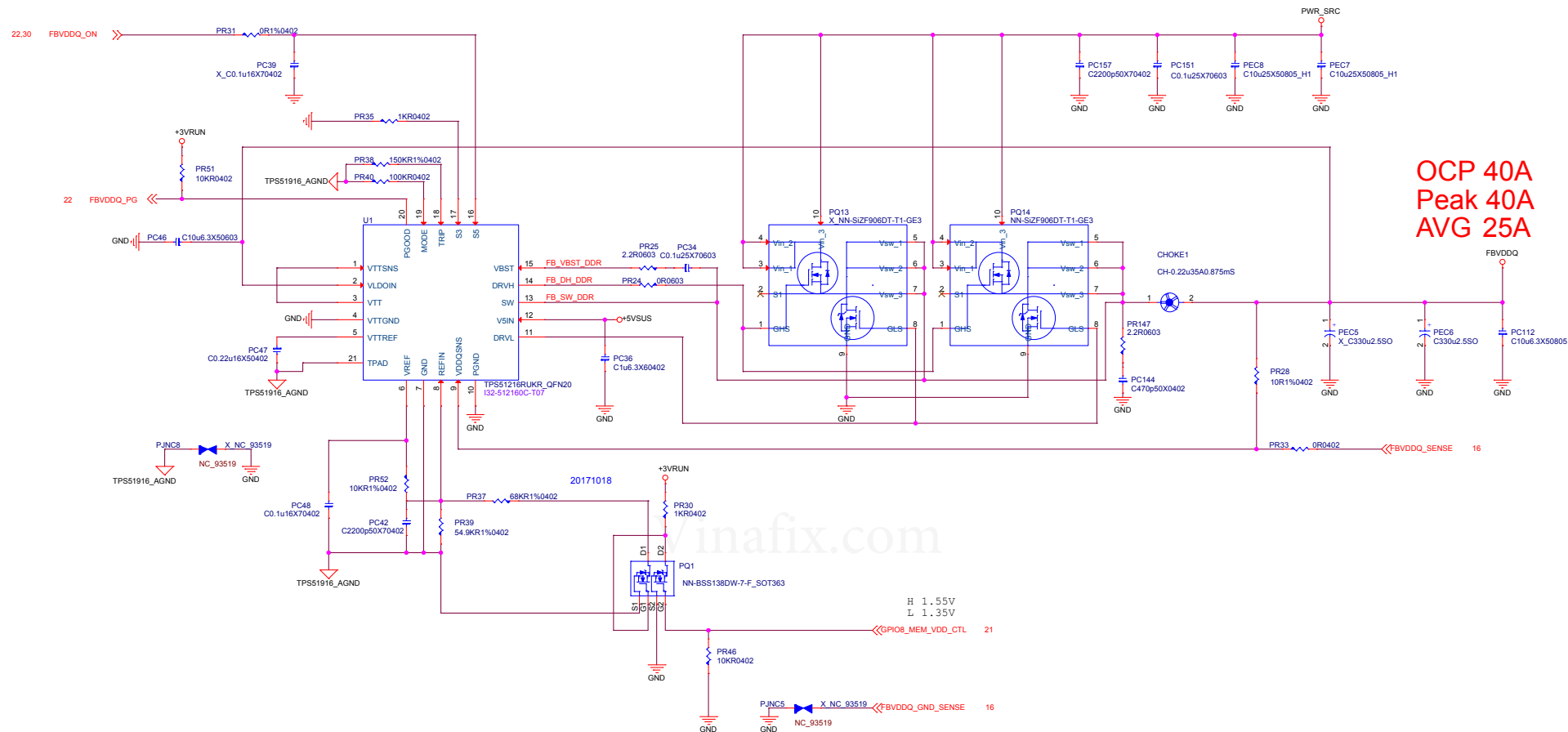


1V8_AON



Voltage = 1.8V
Current = 0.9A

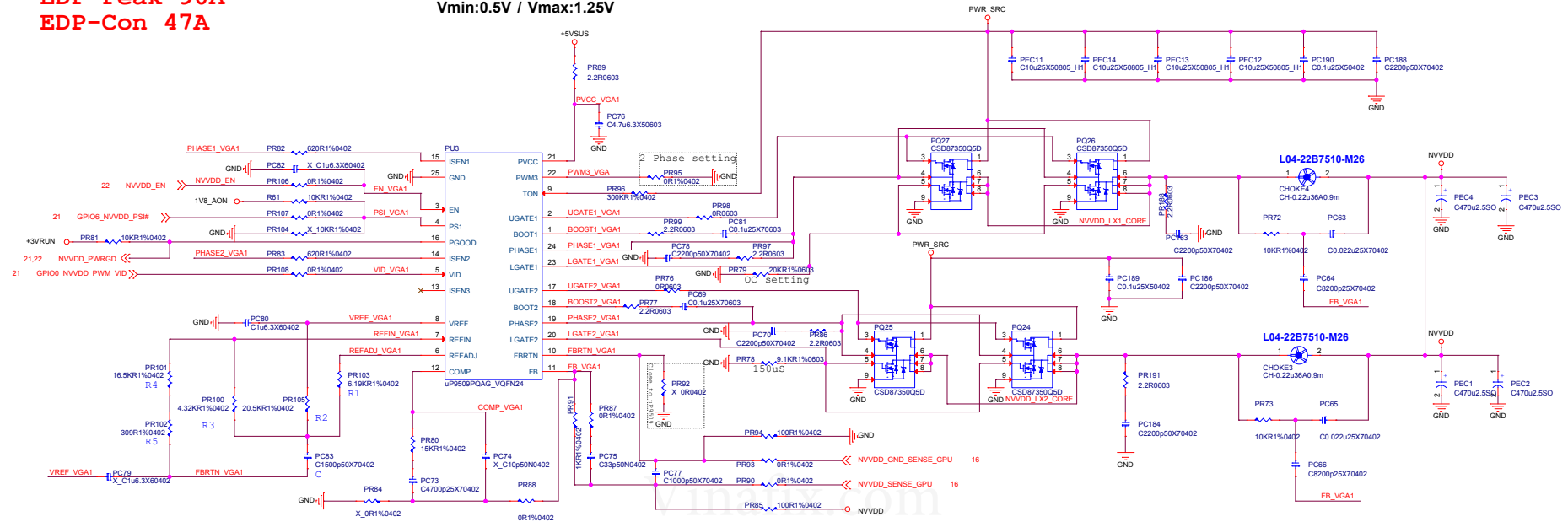
msi MICRO-STAR INT'L CO.,LTD.	
Title	
DGPU POWER PEX VDD/1V8 AON	
Size	Document Number
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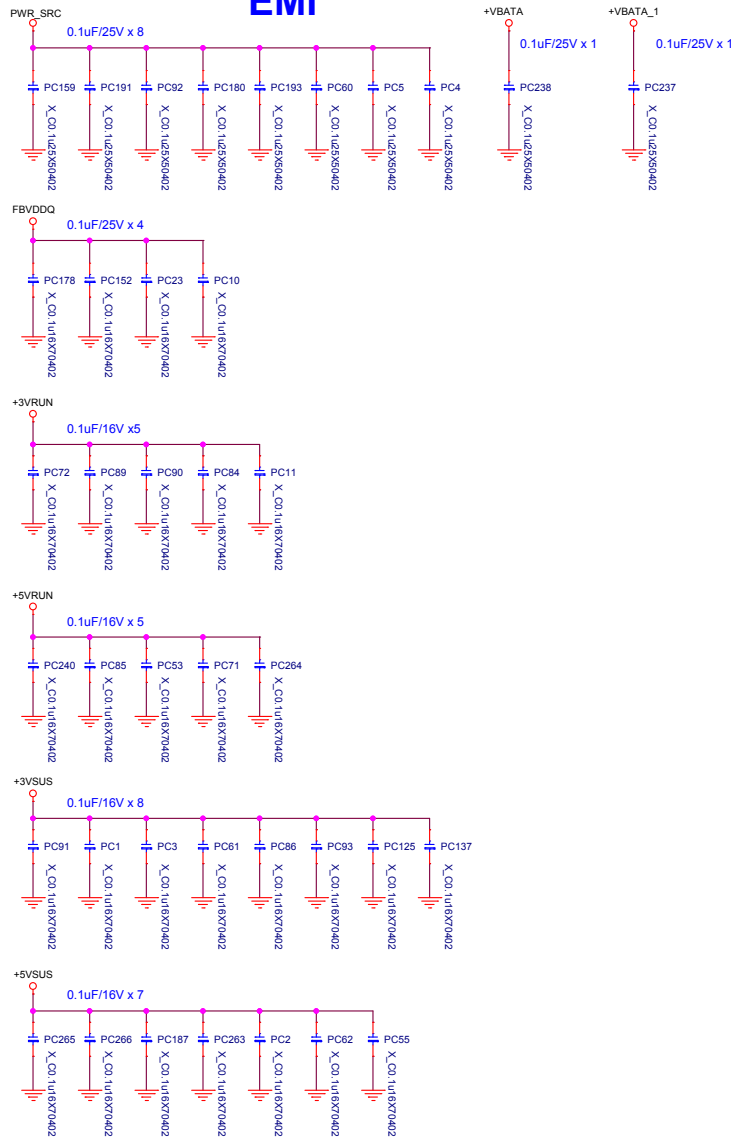
OCP 40A
Peak 40A
AVG 25A

EDP-Peak 90A
EDP-Con 47A

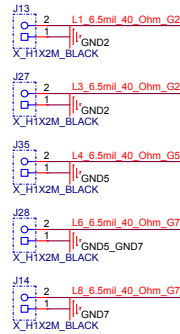
VBoot:0.8V
Vmin:0.5V / Vmax:1.25V



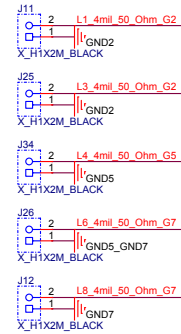
EMI



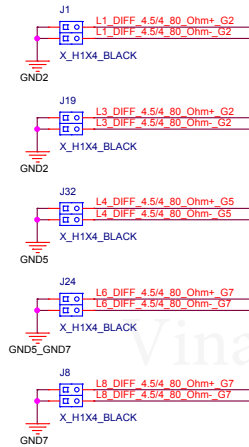
40 OHM Single-End



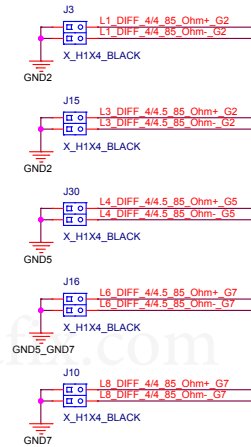
50 OHM Single-End



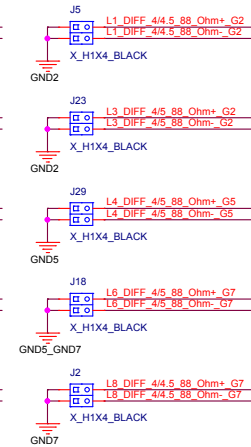
80 OHM Differential



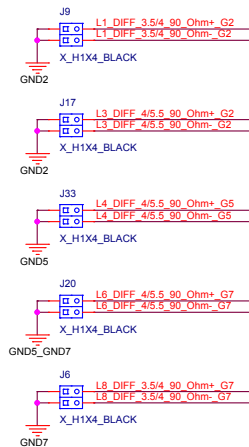
85 OHM Differential



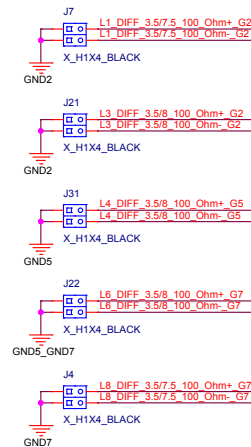
88 OHM Differential

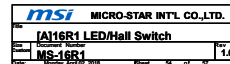


90 OHM Differential

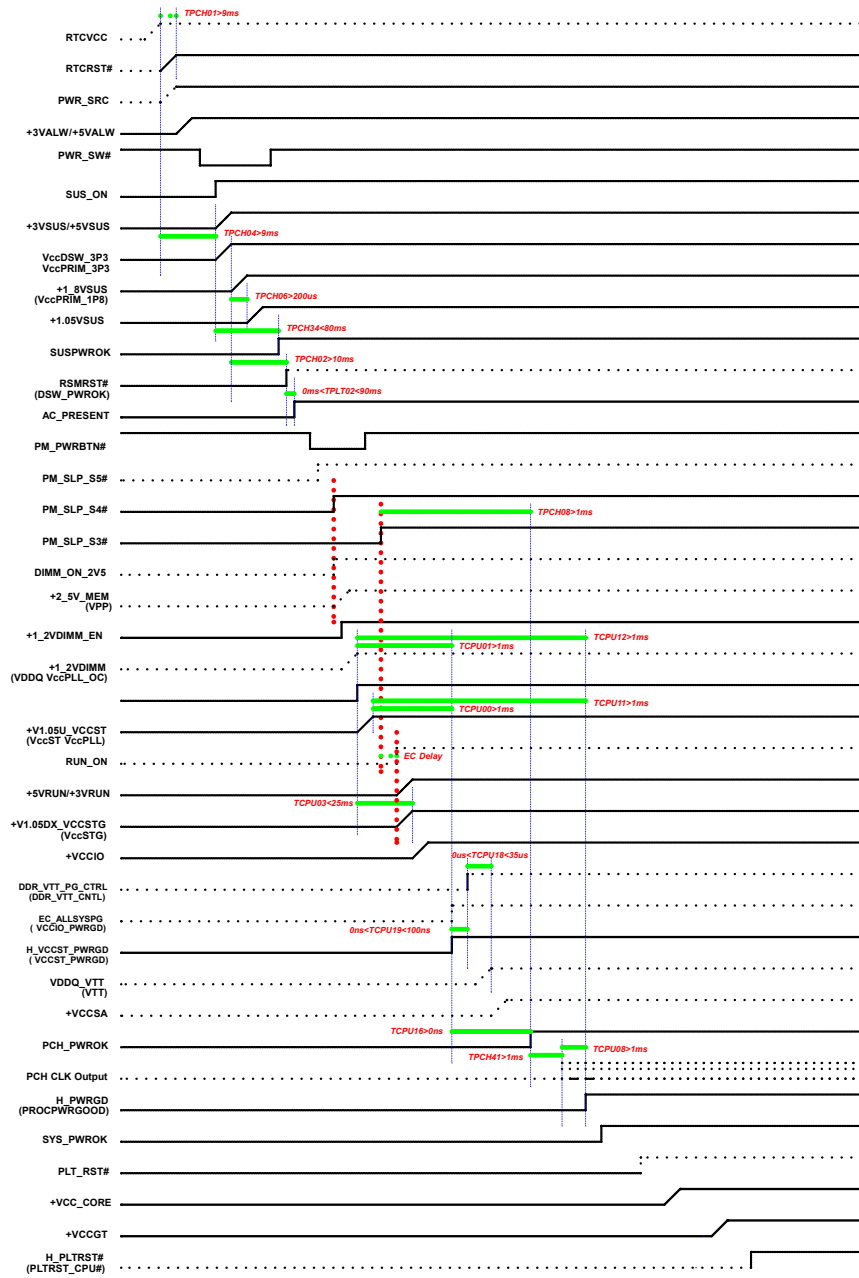


100 OHM Differential

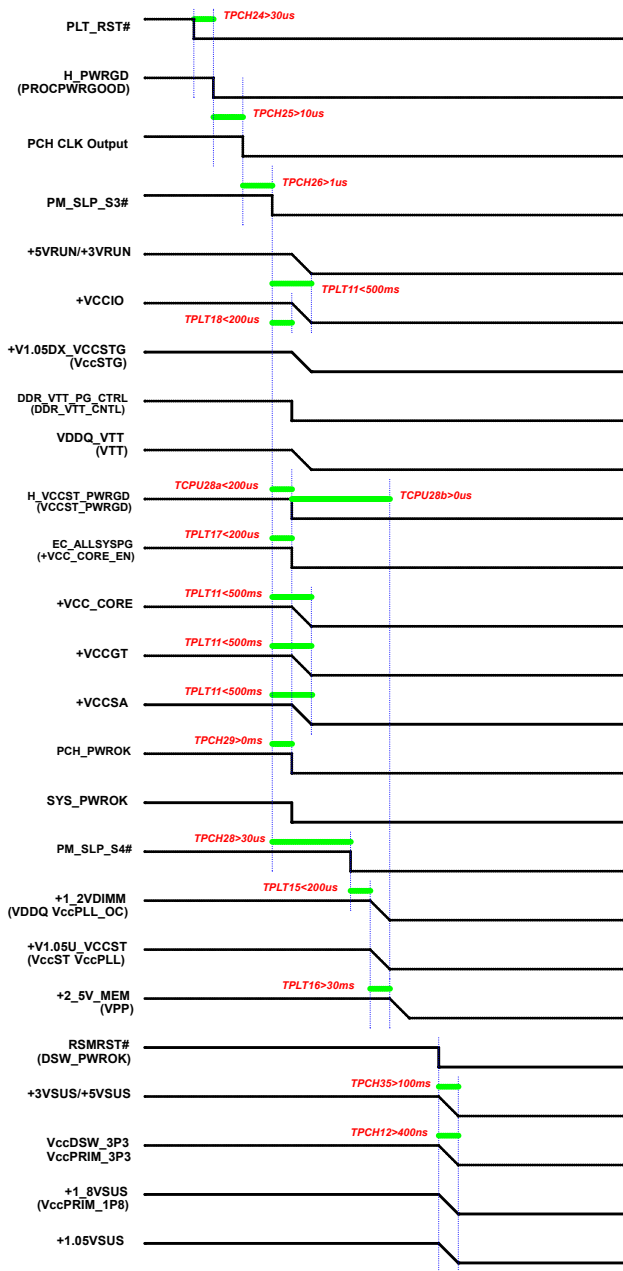




G3 -> S0



S0 -> G3



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